Pratham Ingale

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Education

Georgia Institute of Technology | Atlanta, GA *Expected Graduation: December 2027*
Bachelor of Science in Electrical Engineering, GPA: 4.0

Engineering Experience

SpaceX | Starlink Aviation *September 2025 – December 2025; June 2026 – Present*

Avionics Hardware Design Intern (Summer 2026) ***Woodinville, WA***

- Redesigned **AC- and DC-path input EMI filters** for a **400W aircraft AC/DC PSU**, increasing power capability **38%** while addressing magnetic saturation, thermal limits, and filter impedance. **Passed DO-160 current-harmonics** requirements and led the **EMI/EMC** validation campaign, authoring the test plan and executing **conducted-emissions** testing.
- Led **proton radiation testing** of 4 buck-converter designs with **no DSEE** observed, owning test plans & electrical characterization before owning **schematic & PCB layout** of 4 follow-up coupons for **NSRL heavy-ion** testing of previously **unqualified flight components**.
- Supported critical-path **power and EMI bring-up** for a new antenna revision with 15 new buck converters, reducing **VHF emissions by 15 dB** through switching frequency, operating mode, bootstrap resistor, loop stability, and input filter optimizations.

Avionics Hardware Design Intern (Fall 2025) ***Woodinville, WA***

- Designed a **60W AC/DC isolated half-bridge LLC resonant converter** using soft switching (**ZVS**) to **improve efficiency by 15%** over existing flyback. Tuned the hybrid-hysteretic control loop using **AP310** injection to secure **≥50° phase margin** and **≥20 dB gain margin** across **10–100% load**. Owned schematic & PCB layout; led **bench bring-up**, validating ZVS, resonant-tank behavior, & loop stability.
- Executed staged bring-up of a major **400W** isolated **AC/DC PCBA** design revision across **CrCM PFC, LLC, Boost, & Buck** stages. Validated **PFC current harmonics** to **DO-160** with **PX8000**; characterized efficiency, thermal, & hold-up performance across full load range.
- Led **RCA** for 3 bring-up failures: restored omitted 1V buck-feedback trace (**8.5V runaway**); traced load-switch trips to **chassis-coupled noise**; identified **LLC cross-regulation collapsing** the **auxiliary rail** below converter threshold with main rail unloaded, **rebooting MCU**

Tesla | Cell Manufacturing *May 2025 – August 2025*

Cell Electronics Design Intern ***San Diego, CA***

- Designed a **4kW, 50V/80A mixed-signal PCB** with **1 Mbps CAN FD**, implementing **discrete window-comparator** circuits for automatic CAN termination, hardware addressing, & connector orientation detection. Integrated pre-charge & load-switch soft-start for **inrush control, OCP, & UV/OV protection**. Designed buck & isolated DC power domains with creepage control & **RLC common-mode filters**.
- Engineered **8-layer, 2oz high-current PCB** rated for **2.5kW (500A @ 5V continuous, 570A peak)**; performed **PDN analysis** to optimize current paths & density, via stitching, & copper geometry; led system bring-up & validated power integrity/thermals at **450A for 700s**.
- Designed a **high-speed digital** star interface for **1 host & 2 nodes** with **<3 ns edges** using **controlled-impedance routing**, ground-**via shielding**, interplane capacitive coupling, & **damped RLC filtering**; eliminated 12 transceivers while maintaining signal integrity.

Yellowjacket Space Program | Avionics Hardware Lead *August 2024 – Present*

Recovery System PCB Designer ***Atlanta, GA***

- Designed a mixed-signal recovery PCB with **dual-harness battery feeds**, 2x converter paths with **ideal diode OR-ing**, **3x STM32/EKF** channels with SPI IMU/barometer interfaces & **discrete median voting**; added **4x redundant** safing paths (2x RBF, ESTOP, software)
- Executed **6-layer PCB layout** for 4 buck converters and **10 ignition-driver** channels, **minimizing high di/dt hot-loop** and **return-path inductance** while separating high-current switching from low-voltage control circuitry and maintaining redundant-domain isolation.
- Validated design with **simultaneous** ignition of **10 e-matches** (**300W load step**), identifying a **downstream transient**; increased 48V to 24V buck **crossover** from **22.6kHz to 49.7kHz**, reducing 3.3V transient from **8.2V to 3.9V** and 24V transient from **32.5V to 26.9V**.

RF Link Evaluation PCB Designer ***Atlanta, GA***

- Architected a **4-layer 2.4 GHz mixed-signal RF link** PCB for **LoRa transceiver characterization**, combining switched RF test paths, forward & reverse power measurement, board telemetry, and Compute Module 5 control and data logging over **Ethernet and USB**.
- Designed a **TX-power/VSWR measurement** chain for **0–12 dBm transmit power** & **1.1:1–3:1 VSWR** using a **29.2dB** directional coupler and log detector; bounded forward/reverse inputs to −30 to −17 dBm and −56 to −23 dBm and analyzed **directivity-limited error.**
- Designed **8-channel, 12-bit SAR ADC telemetry** for current, voltage, & temp sensing, including **0–100mA Kelvin-shunt** current sensing, **340Hz anti-alias filters**, & ADC calibration via 1.15V reference; estimated worst-case mux **charge-sharing error** to **~0.10 LSB.**

Skills

Power: Isolated LLC, AC/DC & DC/DC converter design; ZVS/soft switching; loop-gain/stability analysis; EMI filters; PFC & harmonic analysis
Mixed-Signal: I/V/T sensing; SAR ADCs; anti-aliasing/error analysis; comparators & discrete median voters; SPI, I²C, CAN, Ethernet & USB
PCB: PCB stack-up; impedance control & length matching; return-path loop inductance control; creepage; current-density & PDN design
Lab: Oscilloscopes; HV/current probes; e-loads; AP310 FRA; PX8000 power analyzer; IR camera; thermal chambers; power supplies
EDA & Software: Altium Designer, Xpedition Designer, KiCAD, LTspice, SIMPLIS, TINA-TI, Visual Studio Code, GitHub, Enovia, Jira, Excel