Hardware In The Loop

Responsible Engineer: Pratham Ingale

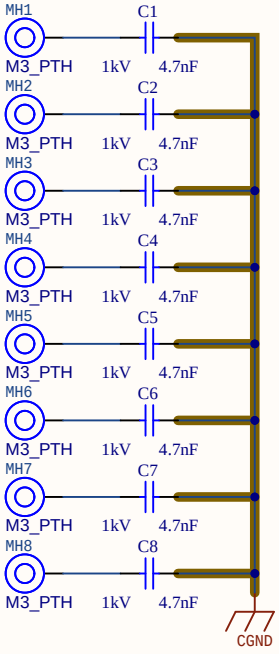
Informational Notes

Layout Notes

Assembly Notes

Software Notes

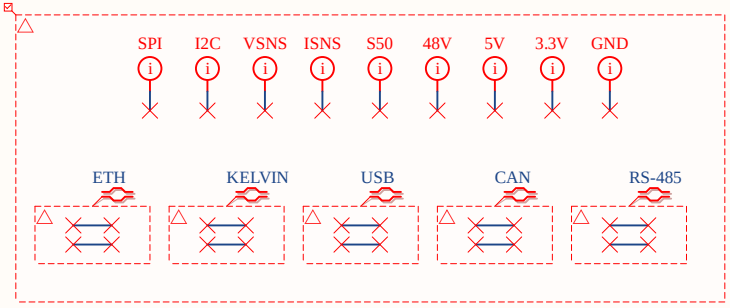
Todo Items



Top Level.SchDoc

Some of these directives have predefined rules in the PCB

Feel free to ignore these



Project: ***Hardware In The Loop_2025-11-11T23_52_26_UTC.PrjPcb***		
Sheet Title: ***Cover Page.SchDoc***		
Size: A4	Schematic Designer: Pratham Ingale PCB Layout Designer: Pratham Ingale Responsible Engineer: Pratham Ingale	*Yellow Jacket Space Program* *Georgia Tech* *Atlanta, GA*
Date: 3/18/2026 Revision: 1.0 Sheet: 1 of: 28		

All calculations are in the HITL folder in sharepoint

Input Power.SchDoc
VOUT
GND
24V0-UNPROT
GND

Input Load Switch.SchDoc
VIN
VOUT
ISNS
VSNS
GND
ISNS_24V0
VSNS_24V0
24V0

48V Boost.SchDoc
VIN
VOUT
48V-DIS
48V-DIS
ISNS
GND
VSNS
GND
ISNS_48V0
VSNS_48V0
48V0

48V Output Load Switch.SchDoc
VIN
VOUT
FSAM-DIS
SHDN
PG
GND
GND
FSAM-PG
48V0-SAM

Output Power.SchDoc
48V0-SAM
24V0-SAM
GND

24V Output Load Switch.SchDoc
VIN
VOUT
GSAM-DIS
SHDN
PG
GND
GND
GSAM-PG
24V0-SAM

5V0-A LDO.SchDoc
VIN
VOUT
GND
GND
5V0-A

5V0-D Buck.SchDoc
VIN
VOUT
ISNS
GND
VSNS
GND
ISNS_5V0-D
VSNS_5V0-D
5V0-D

3V3 LDO.SchDoc
VIN
VOUT
GND
GND
3V3

CM5.SchDoc
VRBF
I2C0
PWRCTRL
SPI0
SPI5
SPI1
DigiPOT_MUX
VRBF
I2C0

PWRCTRL
GPG
FPG
GDIS
FDIS
48DIS
GSAM-PG
FSAM-PG
GSAM-DIS
FSAM-DIS
48V-DIS

SPI
nCS0
nCS1
CIPO
COPI
SCLK

DAC.SchDoc
nCS
CIPO
COPI
SCLK
VOUT0
VOUT1
VOUT2
VOUT3
VOUT4
VOUT5
VOUT6
VOUT7
VDAC_DS
VDAC_CLA
VDAC_CLB
VDAC_RTDC
VDAC_VLVA
VDAC_VLVB
VDAC_TC
VDAC_DET

ADC.SchDoc
nCS
CIPO
COPI
SCLK
AIN0
AIN1
AIN2
AIN3
AIN4
AIN5
AIN6
AIN7
AIN8
AIN9
AINCOM
ISNS_48V0
ISNS_24V0
ISNS_5V0-D
VSNS_48V0
VSNS_5V0-D
VSNS_24V0
VTEST1
VTEST2
GND

ADC.SchDoc
nCS
CIPO
COPI
SCLK
AIN0
AIN1
AIN2
AIN3
AIN4
AIN5
AIN6
AIN7
AIN8
AIN9
AINCOM
ISNS_DET
VSNS_DET
ISNS_VLVA
ISNS_VLVB
VSNS_VLVA
VSNS_VLVB
GND

RTD DigiPOT.SchDoc
nCS
CIPO
COPI
SCLK
I2C0
CAL_RTDA
CAL_RTDB
RTDA
RTDB
VTEST1
VTEST2
RTDA
RTDB
I2C0
VTEST1
VTEST2
CAL_RTDA
CAL_RTDB
DigiPOT_MUX

Differential Sensor.SchDoc
VDAC_DS
VDAC
DIFFSNS
DIFFSNS

Thermocouple.SchDoc
VDAC_TC
VDAC
TC
TCA

Current Loop.SchDoc
VDAC_CLA
VDACA
CLA
CLA
VDAC_CLB
VDACB
CLB
CLB

RTD.SchDoc
VDAC_RTDC
VDAC
RTDC
RTDC

RBF Tag.SchDoc
VRBF
VRBF
RBF
RBF

Valve.SchDoc
VDAC_VLVA
VDACA
VLVA
VLVA
VDAC_VLVB
VDACB
VLVB
VLVB
ISNSA
ISNSB
ISNS_VLVA
ISNS_VLVB
VSNSA
VSNSB
VSNS_VLVA
VSNS_VLVB

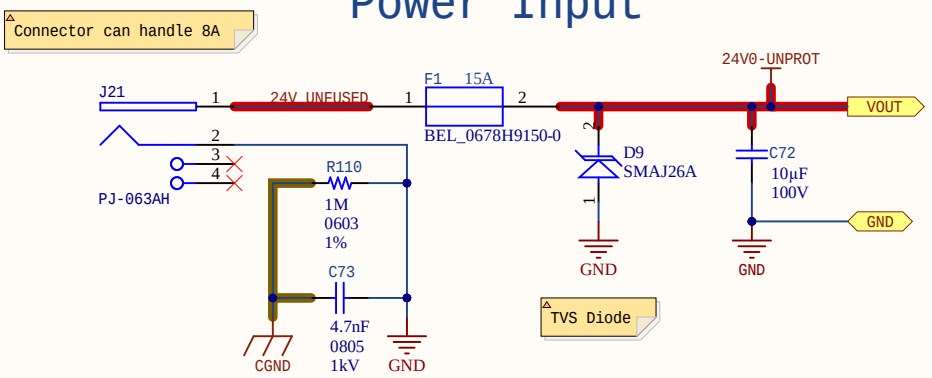
Detonator.SchDoc
VDAC_DET
VDAC
DET
DET
ISNS
ISNS_DET
VSNS
VSNS_DET

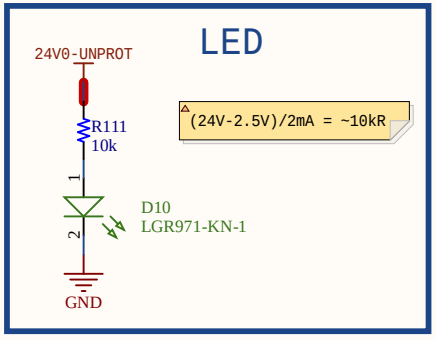
Sig Connectors.SchDoc
DIFFSNS
TCA
CLA
CLB
RTDA
RTDB
RTDC
RBF
VLVA
VLVB
DET
DIFFSNS
TCA
CLA
CLB
RTDA
RTDB
RTDC
RBF
VLVA
VLVB
DET

Project: *Hardware In The Loop_2025-11-11T23_52_26_UTC.PrjPcb*
Sheet Title: *Top Level.SchDoc*

Size: A4	Schematic Designer: Pratham Ingale PCB Layout Designer: Pratham Ingale Responsible Engineer: Pratham Ingale	*Yellow Jacket Space Program* *Georgia Tech* *Atlanta, GA*
Date: 3/18/2026 Revision: 1.0	Sheet: 2 of: 28	

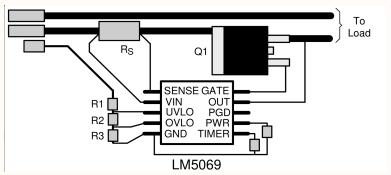
Power Input





Project: ***Hardware In The Loop_2025-11-11T23_52_26_UTC.PrjPcb***		
Sheet Title: ***Input Power.SchDoc***		
Size: A4	Schematic Designer: Pratham Ingale PCB Layout Designer: Pratham Ingale Responsible Engineer: Pratham Ingale	*Yellow Jacket Space Program* *Georgia Tech* *Atlanta, GA*
Date: 3/18/2026 Revision: 1.0 Sheet: 3 of: 28		

Input Load Switch



Add testpoints

TVS Diode is on Input Power sheet

Place C78 close to R112 instead of the VIN pin

7.3A current limit

C75 reduces the CM voltage seen by VIN and SENSE

Place C75 near the NFET's drain

Bulk capacitance

Open drain, pulled low = fault

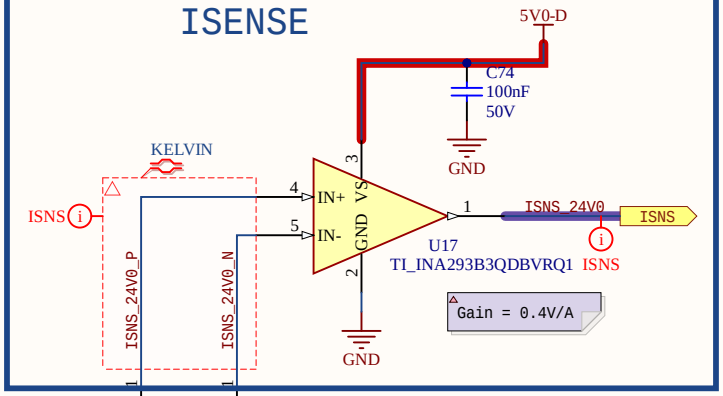
Split into multiple to counteract DC bias

UVLO @ 16.2V
OVLO @ 29.6V

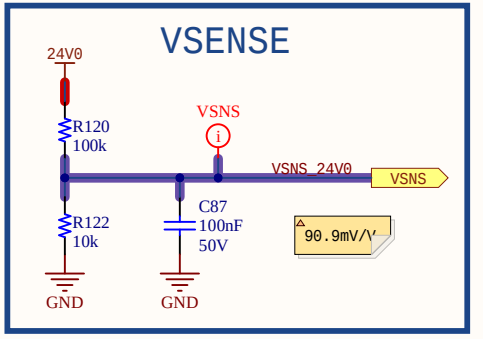
PLIM = 60W
This is a limit of max power dissipation on the FET, not max power output

4.71ms fault timer

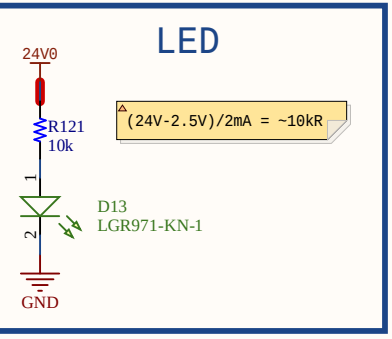
ISENSE



VSENSE



LED

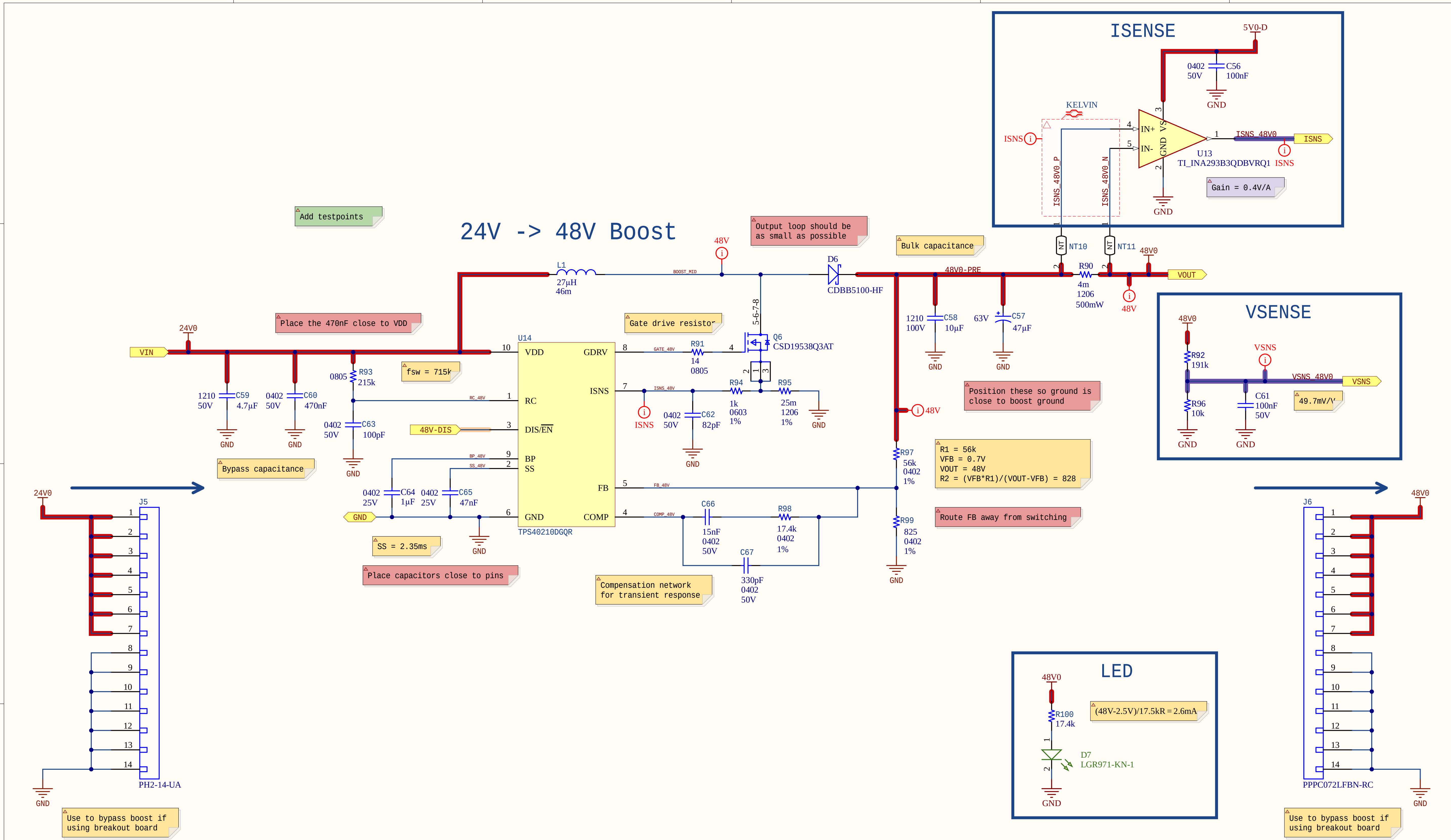


R_{SNS} =	7.5 mΩ
R_{CL1} =	DNP Ω
R_{CL2} =	0 Ω
R_{PWR} =	56 kΩ
C_{TIMER} =	100.00 nF
R1 =	100 kΩ
R2 =	8.66 kΩ
R3 =	10 kΩ
R4 =	N/A kΩ
$C_{dv/dt}$ =	DNP nF
C_{IN} =	0.01 µF
D1	B380-13-F
D2	DNP
Q1	NON-TI MOSFET
#FETs in parallel	1
Q2	DNP
Z1	5.0SMDxx

Design Results	Settings	Units
Current limit	7.3	A
Power Limit	60	W
Circuit Breaker Current	7.3	A
Startup Time	2.76	ms
Insertion Delay	72.7	ms
Fault Timeout	4.71	ms
Restart Time During Fault	940.647	ms
Upper UVLO Threshold	17.998	V
Lower UVLO Threshold	15.898	V
Upper OVLO Threshold	29.665	V
Lower OVLO Threshold	27.383	V

Project: *Hardware In The Loop_2025-11-11T23_52_26_UTC.PrjPcb*
Sheet Title: *Input Load Switch.SchDoc*

Size: A4	Schematic Designer: Peijie Liu PCB Layout Designer: Pratham Ingale Responsible Engineer: Pratham Ingale	*Yellow Jacket Space Program* *Georgia Tech* *Atlanta, GA*
Date: 3/18/2026 Revision: 1.0 Sheet: 4 of: 28		

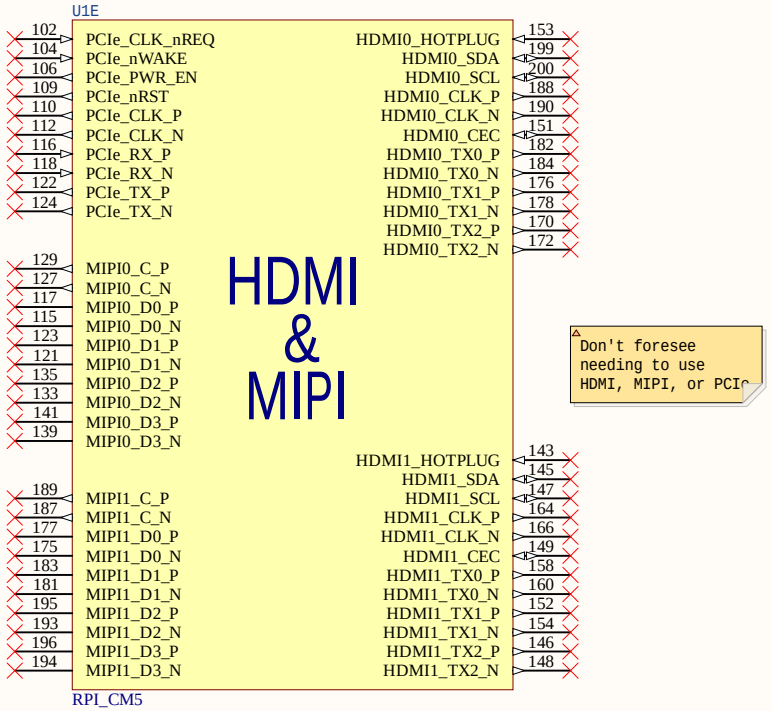

24V -> 48V Boost
Add testpoints
Output loop should be as small as possible
Bulk capacitance
Place the 470nF close to VDD
Gate drive resistor
fsw = 715k
Bypass capacitance
SS = 2.35ms
Place capacitors close to pins
Compensation network for transient response
Position these so ground is close to boost ground
R1 = 56k
VFB = 0.7V
VOUT = 48V
R2 = (VFB*R1)/(VOUT-VFB) = 828
Route FB away from switching
Use to bypass boost if using breakout board
ISENSE
VSENSE
LED
Gain = 0.4V/A
49.7mV/V
(48V-2.5V)/17.5kR = 2.6mA
U14
TPS40210DGQR
VDD
GDRV
RC
ISNS
DIS/EN
BP
SS
FB
GND
COMP
L1
27µH
46m
D6
CDBB5100-HF
Q6
CSD19538Q3AT
U13
TI_INA293B3QDBVRQ1
KELVIN
D7
LGR971-KN-1
J5
PH2-14-UA
J6
PPPC072LFBN-RC
VIN
VOUT
ISNS
VSNS
48V-DIS
24V0
48V0
48V0-PRE
5V0-D
48V
GND
C59 1210 50V 4.7µF
C60 0402 50V 470nF
R93 0805 215k
C63 0402 50V 100pF
C64 0402 25V 1µF
C65 0402 25V 47nF
R91 14 0805
R94 1k 0603 1%
R95 25m 1206 1%
C62 0402 50V 82pF
C66 15nF 0402 50V
R98 17.4k 0402 1%
C67 330pF 0402 50V
C58 1210 100V 10µF
C57 63V 47µF
R90 4m 1206 500mW
R97 56k 0402 1%
R99 825 0402 1%
C56 0402 50V 100nF
NT10
NT11
R92 191k
R96 10k
C61 100nF 50V
R100 17.4k

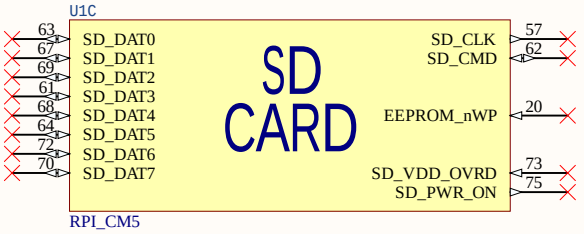
Project: *Hardware In The Loop_2025-11-11T23_52_26_UTC.PrjPcb*
Sheet Title: *48V Boost.SchDoc*

Size: A4
Schematic Designer: Pratham Ingale
PCB Layout Designer: Pratham Ingale
Responsible Engineer: Pratham Ingale

Yellow Jacket Space Program
Georgia Tech
Atlanta, GA

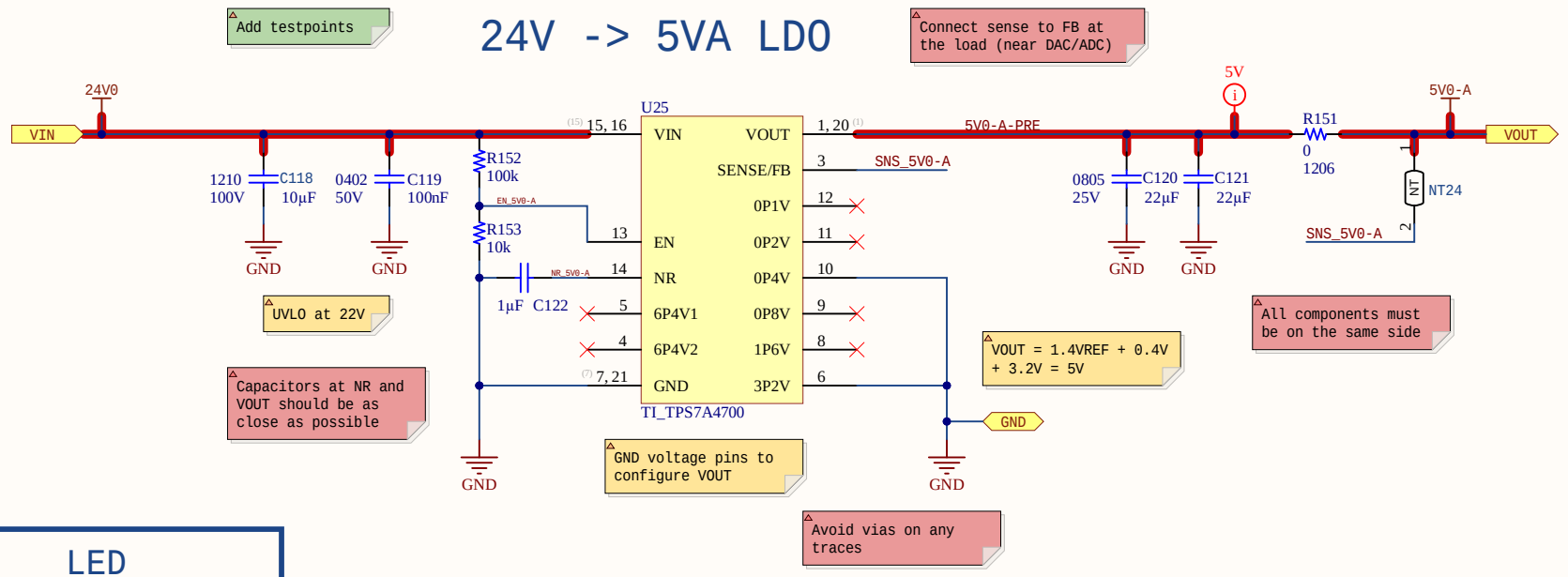
Date: 3/18/2026 Revision: 1.0 Sheet: 5 of: 28



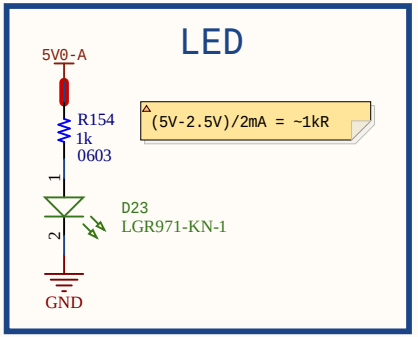


Project: *Hardware In The Loop_2025-11-11T23_52_26_UTC.PrjPcb*		
Sheet Title: *CM5 Unused.SchDoc*		
Size: A4	Schematic Designer: Pratham Ingale PCB Layout Designer: Pratham Ingale Responsible Engineer: Pratham Ingale	*Yellow Jacket Space Program* *Georgia Tech* *Atlanta, GA*
Date: 3/18/2026 Revision: 1.0 Sheet: 6 of: 7		

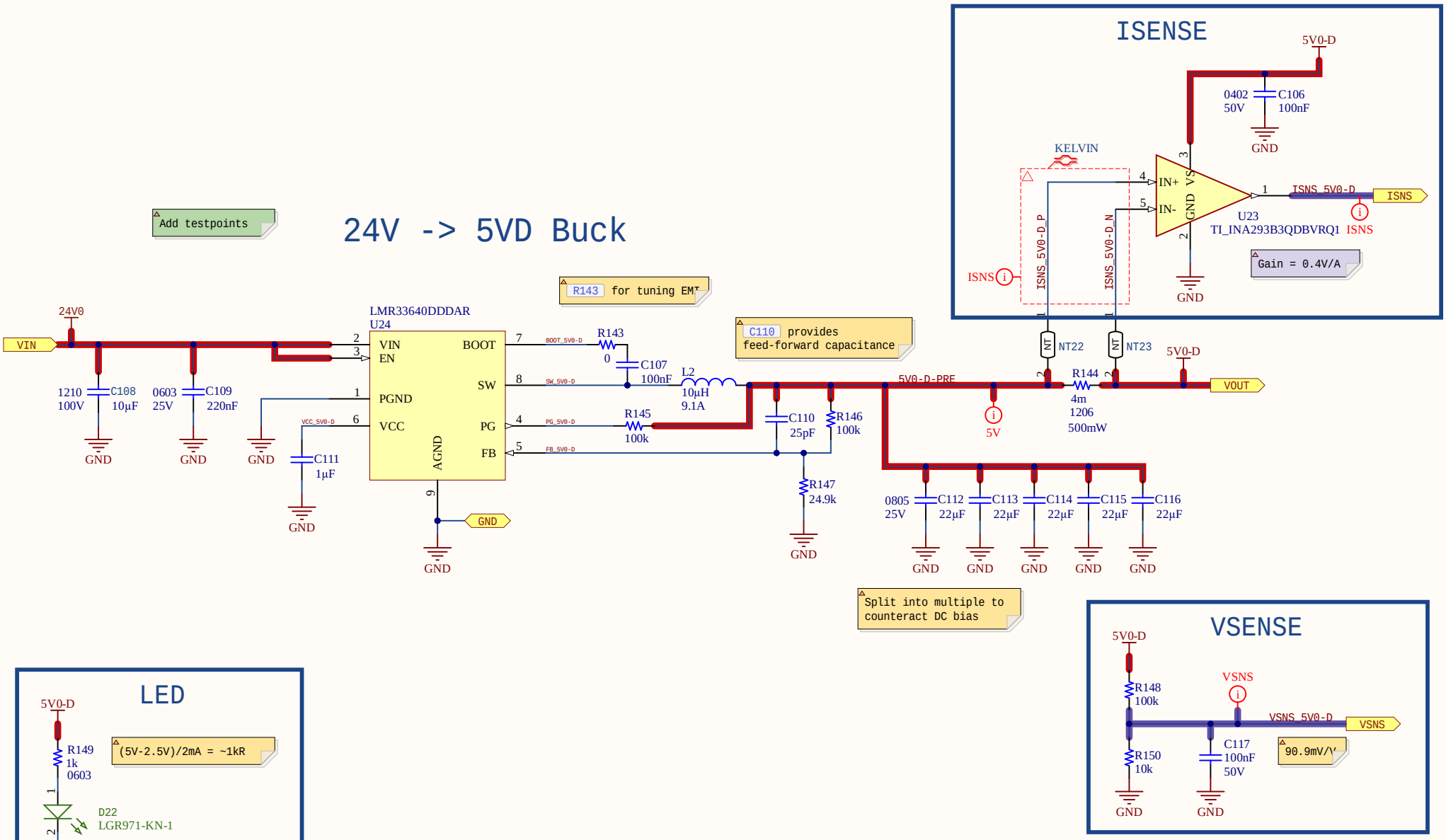
24V -> 5VA LDO



LED

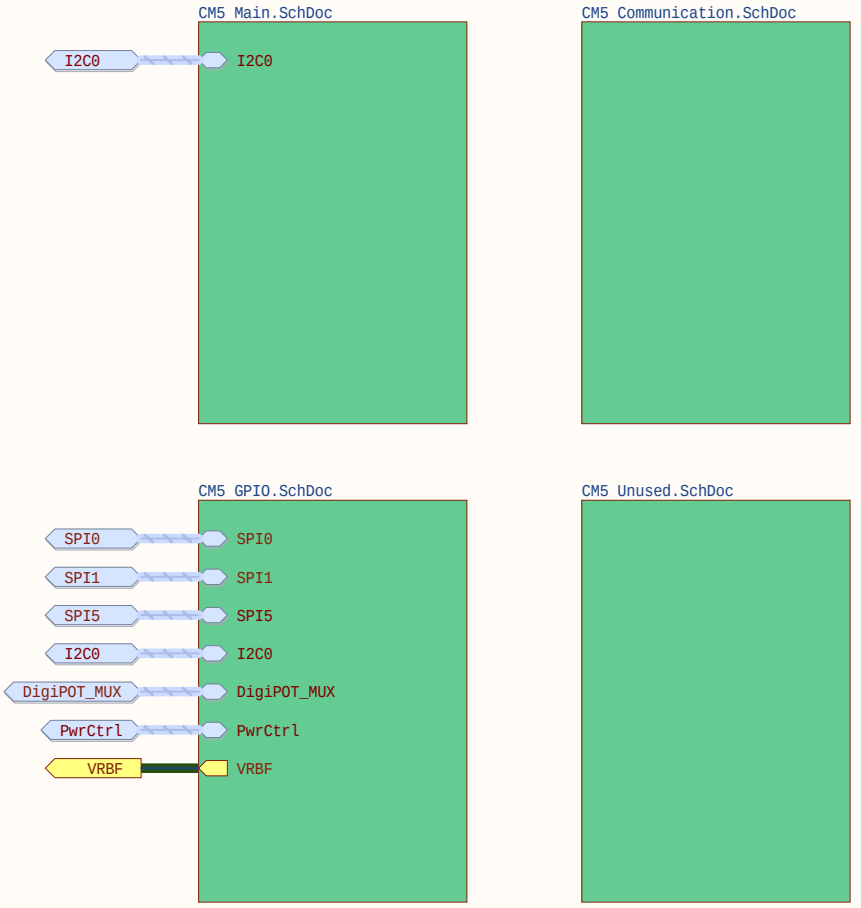


Project: *Hardware In The Loop_2025-11-11T23_52_26_UTC.PrjPcb*		
Sheet Title: *5V0-A LDO.SchDoc*		
Size: A4	Schematic Designer: Pratham Ingale PCB Layout Designer: Pratham Ingale Responsible Engineer: Pratham Ingale	*Yellow Jacket Space Program* *Georgia Tech* *Atlanta, GA*
Date: 3/18/2026 Revision: 1.0 Sheet: 6 of: 28		



Project: *Hardware In The Loop_2025-11-11T23_52_26_UTC.PrjPcb*		
Sheet Title: *5V0-D Buck.SchDoc*		
Size: A4	Schematic Designer: Mitchell Jiang PCB Layout Designer: Pratham Ingale Responsible Engineer: Pratham Ingale	*Yellow Jacket Space Program* *Georgia Tech* *Atlanta, GA*
Date: 3/18/2026 Revision: 1.0 Sheet: 7 of: 28		

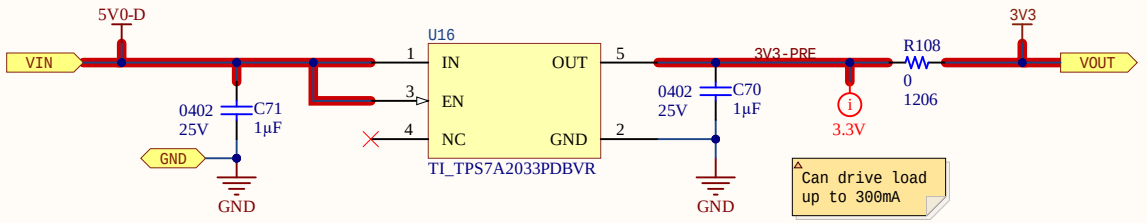
Compute Module 5



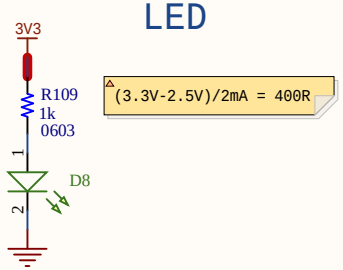
Project: *Hardware In The Loop_2025-11-11T23_52_26_UTC.PrjPcb*		
Sheet Title: *CM5.SchDoc*		
Size: A4	Schematic Designer: Pratham Ingale PCB Layout Designer: Pratham Ingale Responsible Engineer: Pratham Ingale	*Yellow Jacket Space Program* *Georgia Tech* *Atlanta, GA*
Date: 3/18/2026 Revision: 1.0 Sheet: 9 of: 28		

Add testpoints

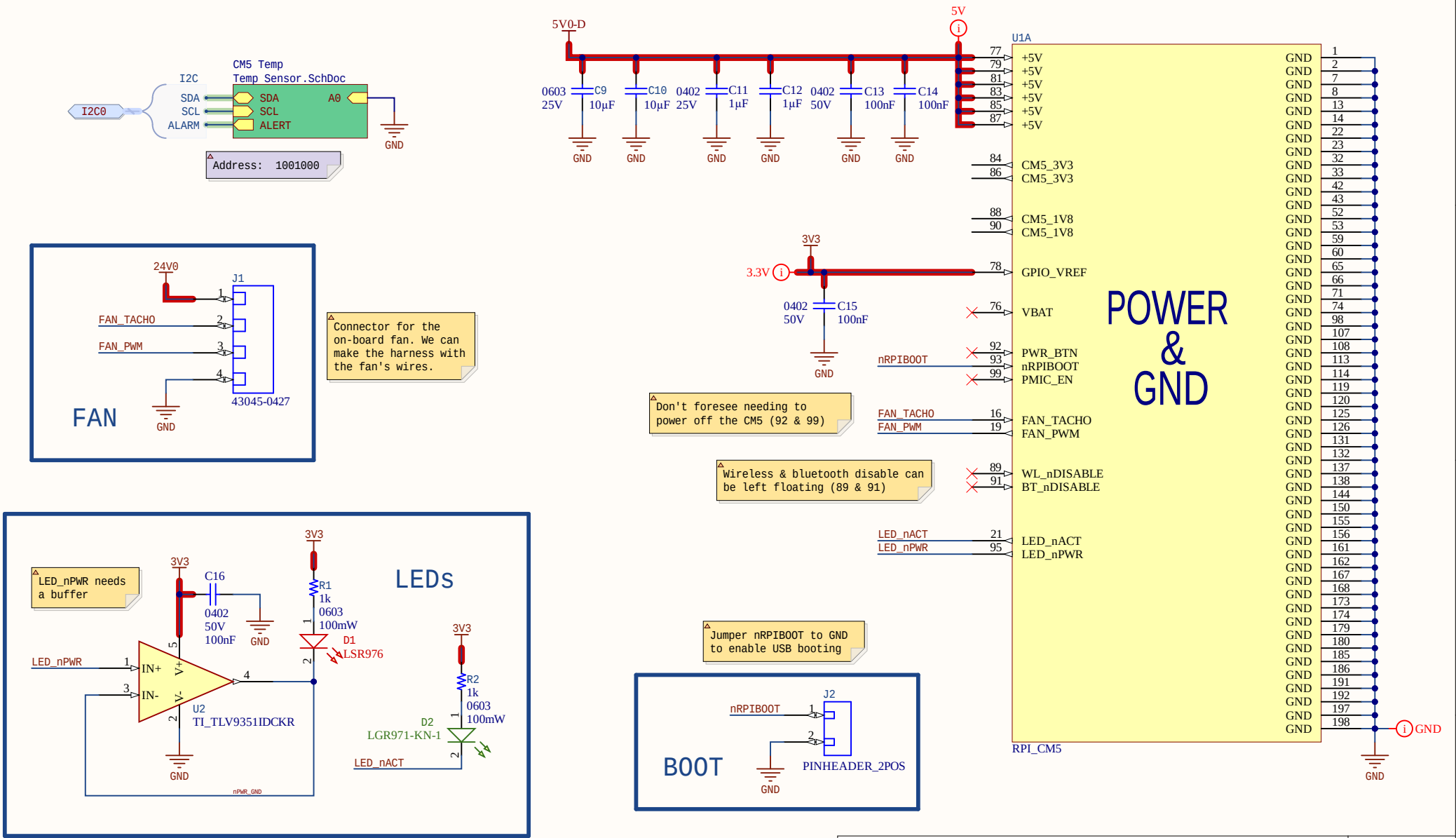
5VD -> 3V3 LDO



LED

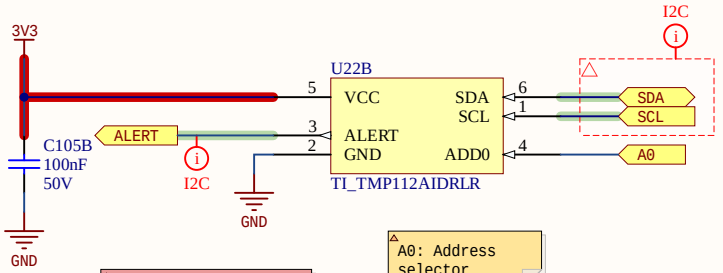


Project: ***Hardware In The Loop_2025-11-11T23_52_26_UTC.PrjPcb***		
Sheet Title: ***3V3 LDO.SchDoc***		
Size: A4	Schematic Designer: Pratham Ingale PCB Layout Designer: Pratham Ingale Responsible Engineer: Pratham Ingale	*Yellow Jacket Space Program* *Georgia Tech* *Atlanta, GA*
Date: 3/18/2026 Revision: 1.0 Sheet: 9 of: 28		



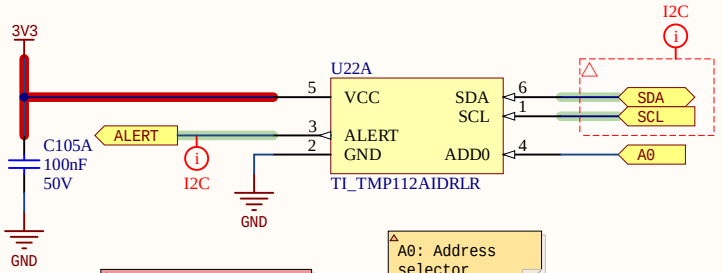
Project: *Hardware In The Loop_2025-11-11T23_52_26_UTC.PrjPcb*			
Sheet Title: *CM5 Main.SchDoc*			
Size: A4	Schematic Designer: Pratham Ingale PCB Layout Designer: Pratham Ingale Responsible Engineer: Pratham Ingale	*Yellow Jacket Space Program* *Georgia Tech* *Atlanta, GA*	
Date: 3/18/2026	Revision: 1.0	Sheet: 10 of: 28	

I2C Temperature Sensor



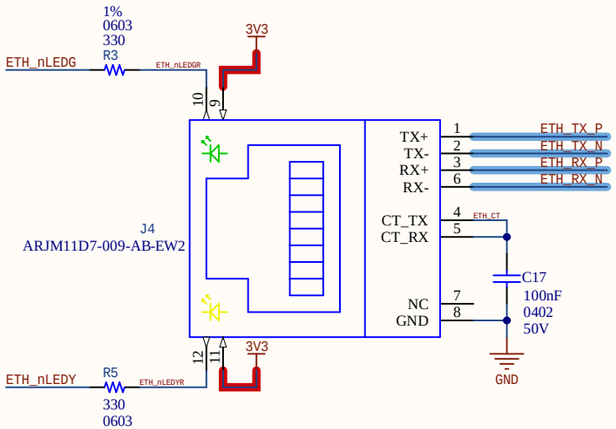
Project: *Hardware In The Loop_2025-11-11T23_52_26_UTC.PrjPcb*		
Sheet Title: *Temp Sensor.SchDoc*		
Size: A4	Schematic Designer: Peijie Liu PCB Layout Designer: Pratham Ingale Responsible Engineer: Pratham Ingale	*Yellow Jacket Space Program* *Georgia Tech* *Atlanta, GA*
Date: 3/18/2026 Revision: 1.0 Sheet: 11 of: 28		

I2C Temperature Sensor

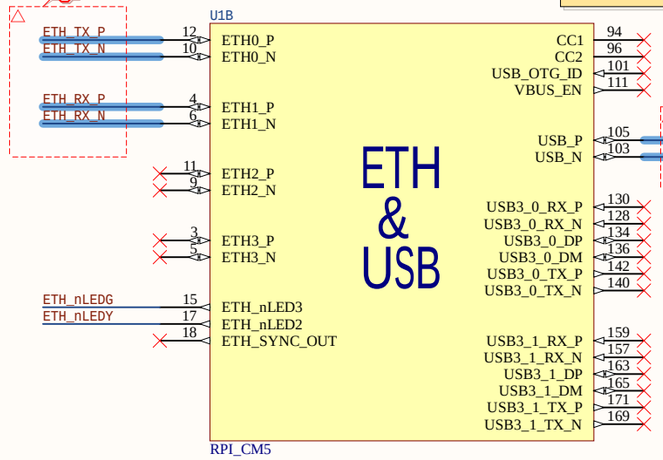


Project: *Hardware In The Loop_2025-11-11T23_52_26_UTC.PrjPcb*		
Sheet Title: *Temp Sensor.SchDoc*		
Size: A4	Schematic Designer: Peijie Liu PCB Layout Designer: Pratham Ingale Responsible Engineer: Pratham Ingale	*Yellow Jacket Space Program* *Georgia Tech* *Atlanta, GA*
Date: 3/18/2026 Revision: 1.0 Sheet: 11 of: 28		

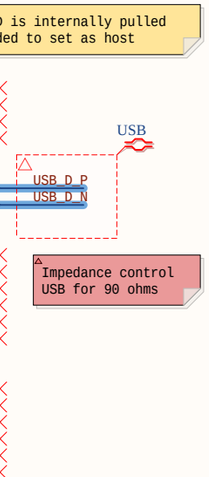
ETHERNET



Impedance control
ETH for 100 ohms

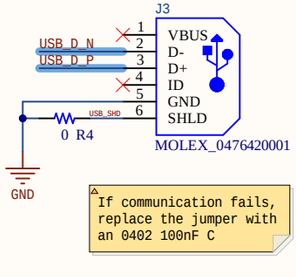


USB_OTG_ID is internally pulled up, grounded to set as host

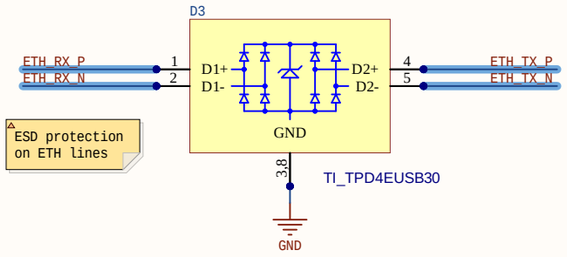


Impedance control
USB for 90 ohms

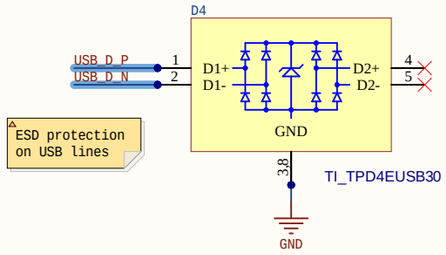
When flashing with USB, ensure the jumper on nRPIBOOT is on



If communication fails, replace the jumper with an 0402 100nF C

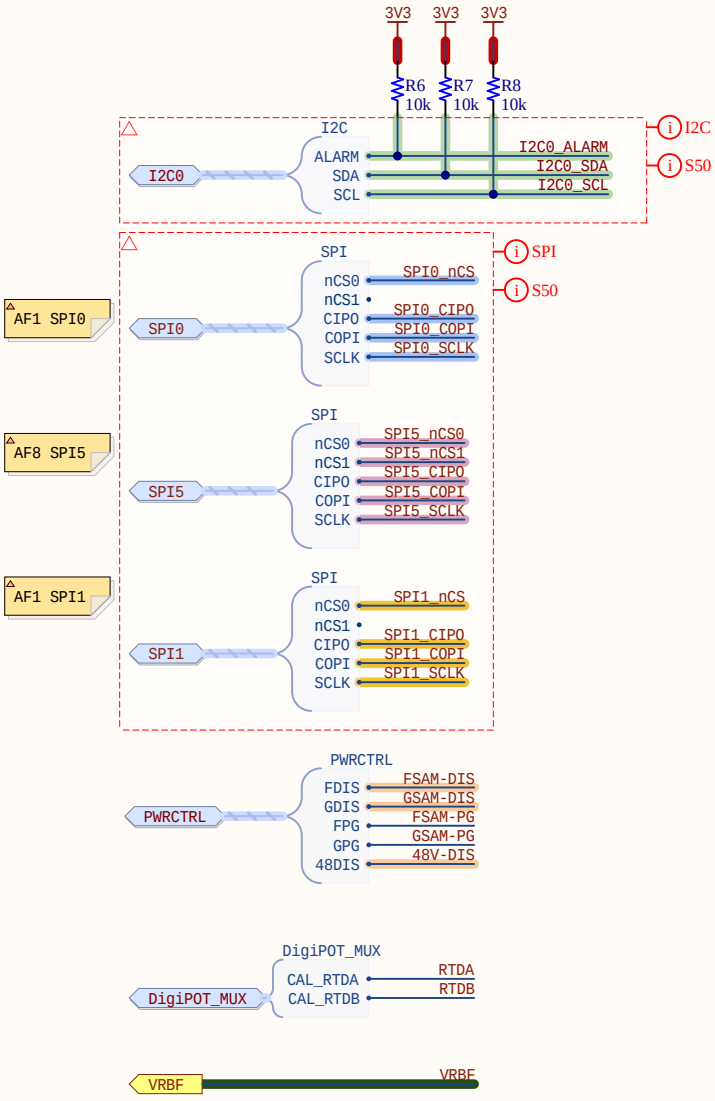


ESD protection on ETH lines



ESD protection on USB lines

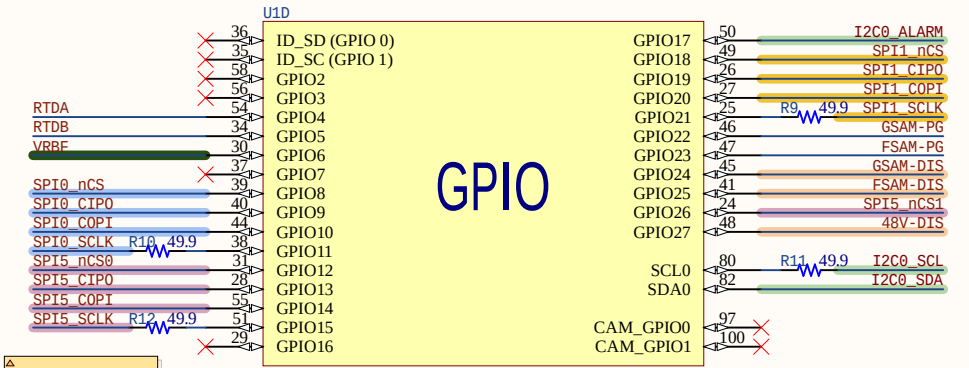
Project: *Hardware In The Loop_2025-11-11T23_52_26_UTC.PrjPcb*			
Sheet Title: *CM5 Communication.SchDoc*			
Size: A4	Schematic Designer: Pratham Ingale PCB Layout Designer: Pratham Ingale Responsible Engineer: Pratham Ingale	*Yellow Jacket Space Program* *Georgia Tech* *Atlanta, GA*	YJSP
Date: 3/18/2026	Revision: 1.0	Sheet: 12 of: 28	



Impedance control for 50 ohms

GPIO	Function Chosen	Description	FUNC	Color Key
0		HAT ID		SPI0
1		HAT ID		SPI1
2		1.8k PullUp		SPI5
3		1.8k PullUp		General GPIO
4	CAL_RTDA	OUT		I2C
5	CAL_RTDB	OUT		
6	VRBF	OUT		
7				
8	SPI0 CSn[0]	DAC	AF0	
9	SPI0 SIO[1]	CIPO		
10	SPI0 SIO[0]	COPI		
11	SPI0 SCLK	SCLK		
12	SPI5 CSn[0]	ADC1	AF8	
13	SPI5 SIO[1]	CIPO		
14	SPI5 SIO[0]	COPI		
15	SPI5 SCLK	SCLK		
16				
17	I2C0 Alarm			
18	SPI1CSn[0]	RTD_DigiPOT	AF0	
19	SPI1 SIO[1]	CIPO		
20	SPI1 SIO[0]	COPI		
21	SPI1 SCLK	SCLK		
22	GSAM-PG	IN		
23	FSAM-PG	IN		
24	GSAM-DIS	OUT		
25	FSAM-DIS	OUT		
26	SPI5 CSn[1]	ADC2		
27	48V-DIS	OUT		
38(SDA0)	I2C0 SDA	MIPI	Fixed	
39(SCL0)	I2C0 SCL	MIPI	Fixed	

GPIO0: HAT ID
GPIO1: HAT ID
GPIO2: 1.8k pulled_up
GPIO3: 1.8k pulled_up

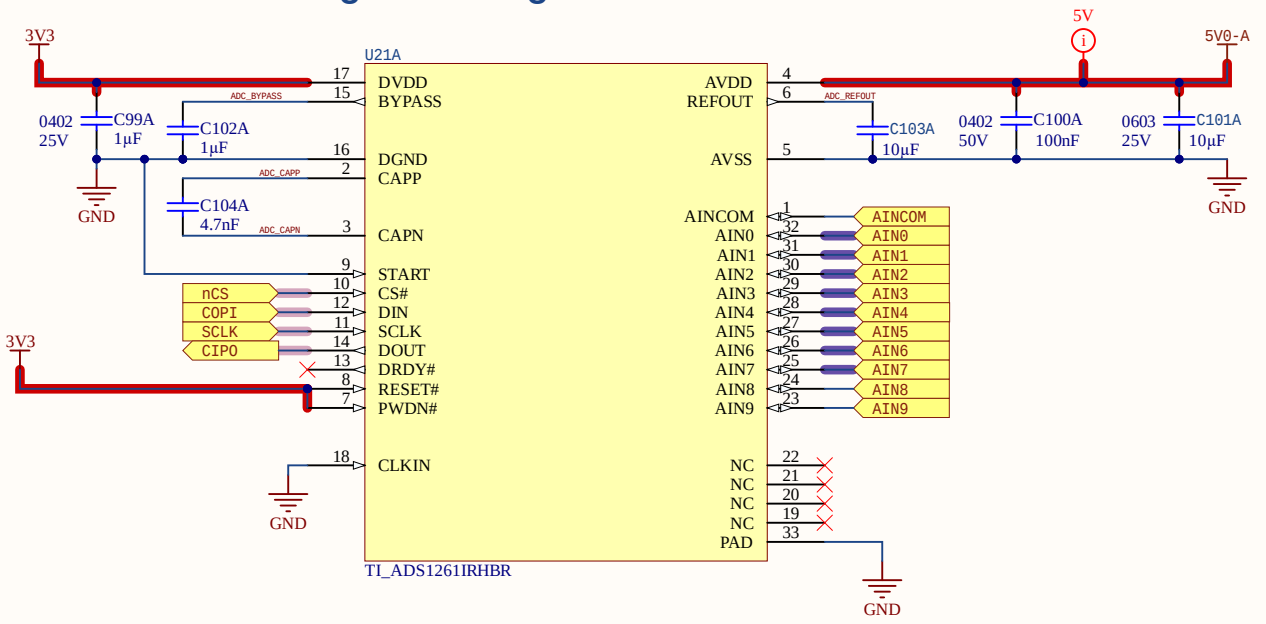


50R to reduce ringing

Place resistors close to driving source

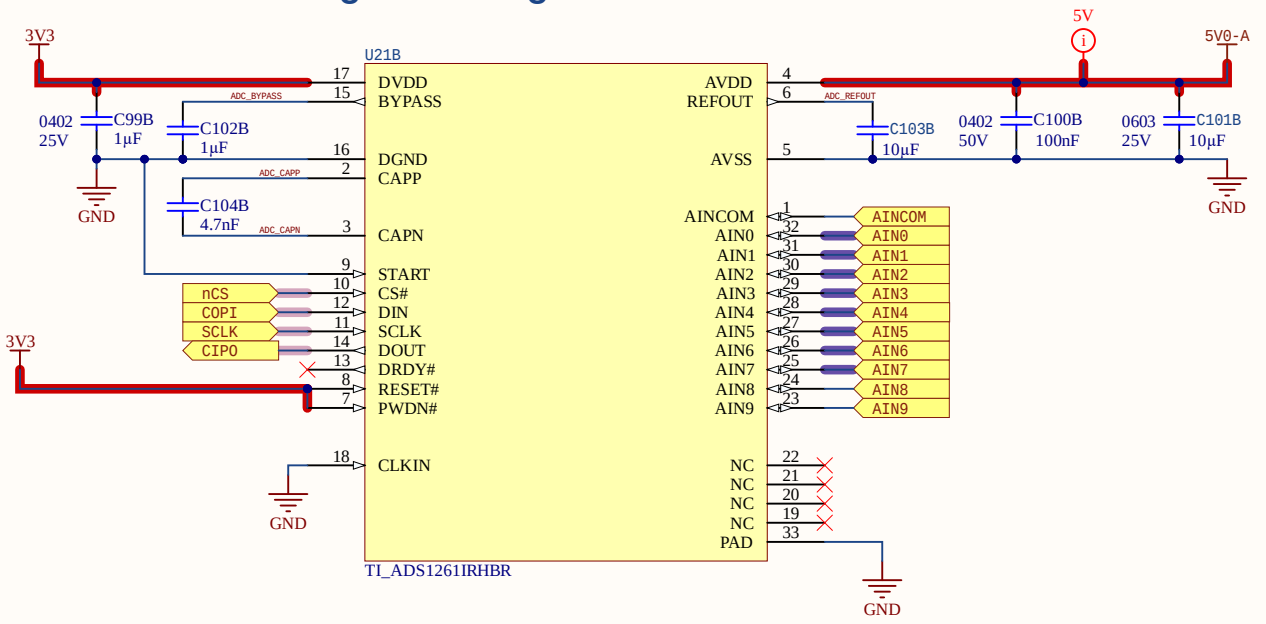
Project: *Hardware In The Loop_2025-11-11T23_52_26_UTC.PrjPcb*		
Sheet Title: *CM5 GPIO.SchDoc*		
Size: A4	Schematic Designer: Pratham Ingale PCB Layout Designer: Pratham Ingale Responsible Engineer: Pratham Ingale	*Yellow Jacket Space Program* *Georgia Tech* *Atlanta, GA*
Date: 3/18/2026 Revision: 1.0 Sheet: 13 of: 28		

Analog to Digital Converter



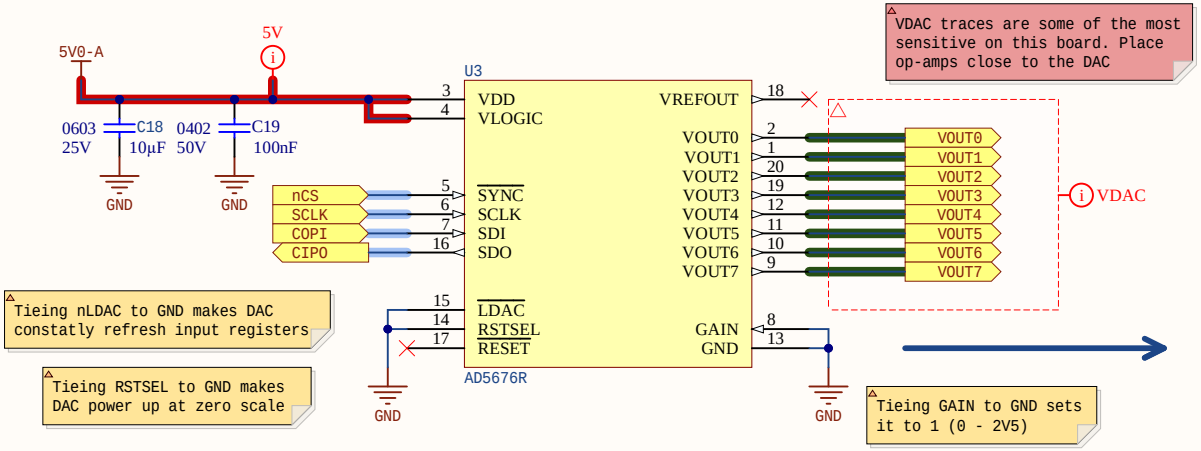
Project: ***Hardware In The Loop_2025-11-11T23_52_26_UTC.PrjPcb***		
Sheet Title: ***ADC.SchDoc***		
Size: A4	Schematic Designer: Pratham Ingale PCB Layout Designer: Pratham Ingale Responsible Engineer: Pratham Ingale	*Yellow Jacket Space Program* *Georgia Tech* *Atlanta, GA*
Date: 3/18/2026 Revision: 1.0 Sheet: 15 of: 28		

Analog to Digital Converter



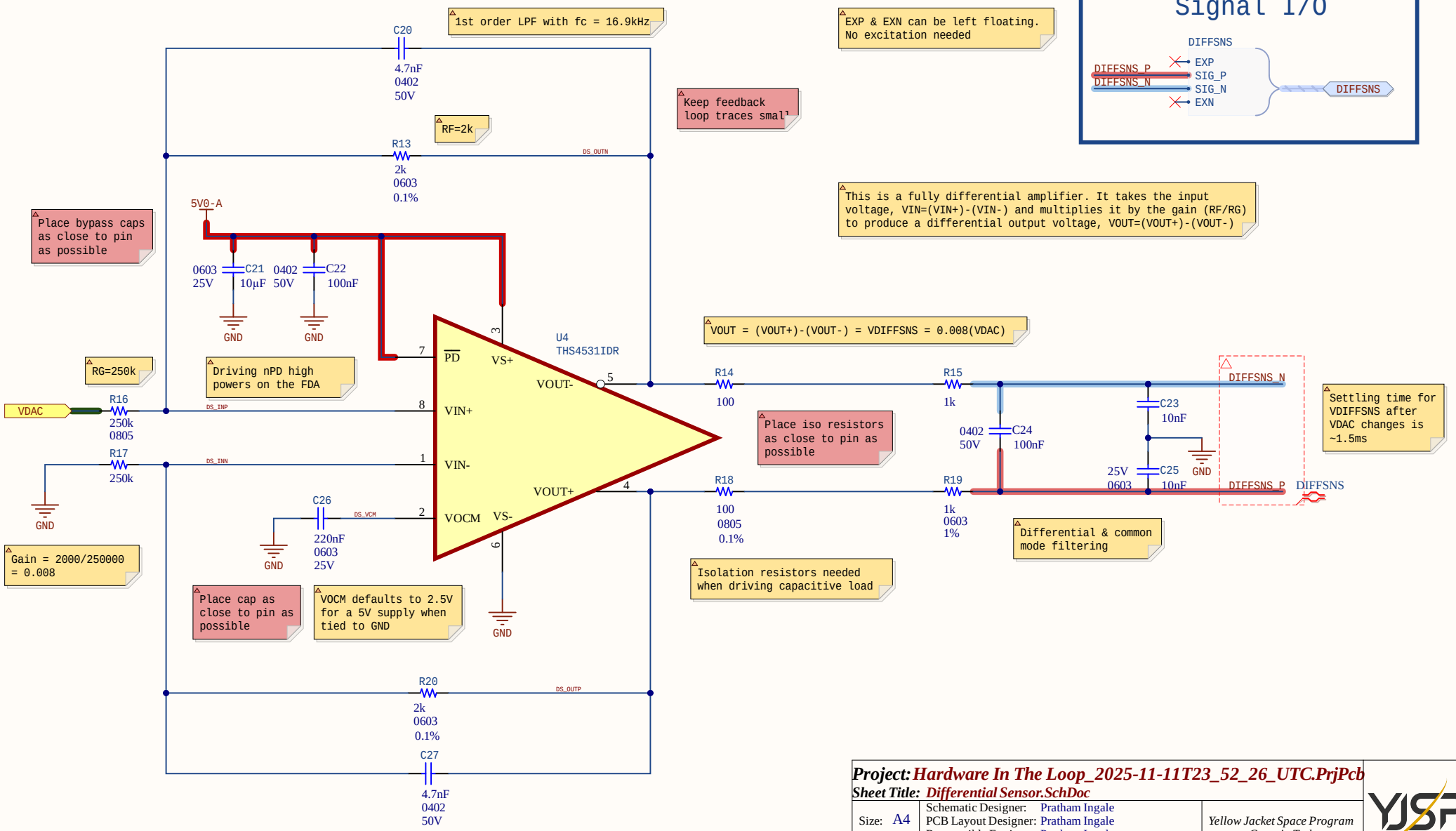
Project: *Hardware In The Loop_2025-11-11T23_52_26_UTC.PrjPcb*		
Sheet Title: *ADC.SchDoc*		
Size: A4	Schematic Designer: Pratham Ingale PCB Layout Designer: Pratham Ingale Responsible Engineer: Pratham Ingale	*Yellow Jacket Space Program* *Georgia Tech* *Atlanta, GA*
Date: 3/18/2026 Revision: 1.0 Sheet: 15 of: 28		

Digital to Analog Converter



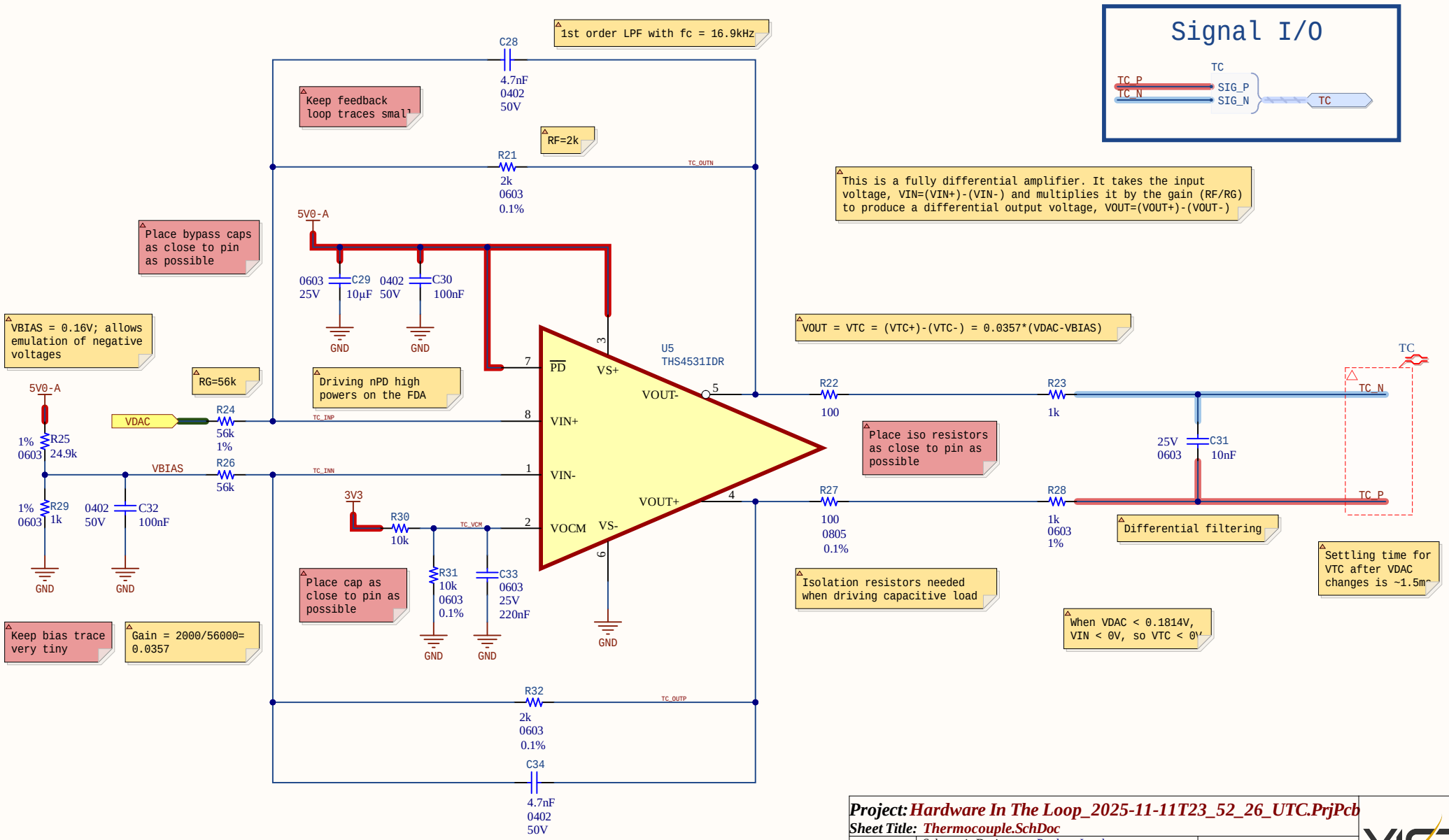
Project: *Hardware In The Loop_2025-11-11T23_52_26_UTC.PrjPcb*		
Sheet Title: *DAC.SchDoc*		
Size: A4	Schematic Designer: Pratham Ingale PCB Layout Designer: Pratham Ingale Responsible Engineer: Pratham Ingale	*Yellow Jacket Space Program* *Georgia Tech* *Atlanta, GA*
Date: 3/18/2026 Revision: 1.0 Sheet: 16 of: 28		

Differential Sensor Emulation



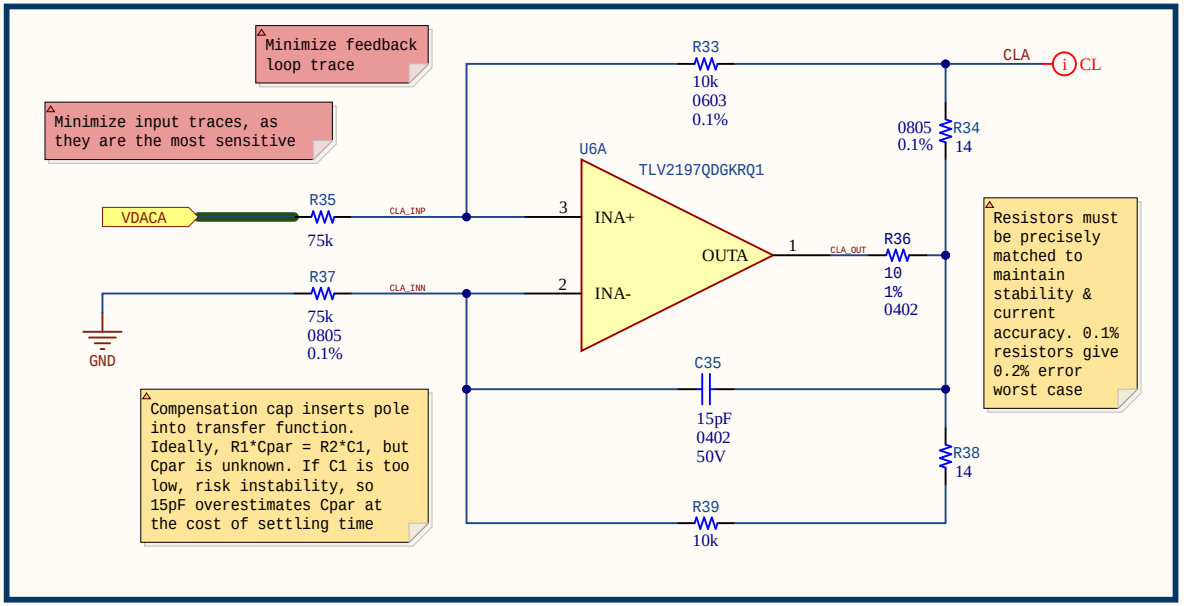
Project: *Hardware In The Loop_2025-11-11T23_52_26_UTC.PrjPcb*		
Sheet Title: *Differential Sensor.SchDoc*		
Size: A4	Schematic Designer: Pratham Ingale PCB Layout Designer: Pratham Ingale Responsible Engineer: Pratham Ingale	*Yellow Jacket Space Program* *Georgia Tech* *Atlanta, GA*
Date: 3/18/2026 Revision: 1.0 Sheet: 17 of: 28		

Thermocouple Emulation



Project: *Hardware In The Loop_2025-11-11T23_52_26_UTC.PrjPcb*		
Sheet Title: *Thermocouple.SchDoc*		
Size: A4	Schematic Designer: Pratham Ingale PCB Layout Designer: Pratham Ingale Responsible Engineer: Pratham Ingale	*Yellow Jacket Space Program* *Georgia Tech* *Atlanta, GA*
Date: 3/18/2026 Revision: 1.0 Sheet: 18 of: 28		

Current Loop Sensor Emulation

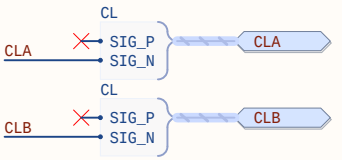


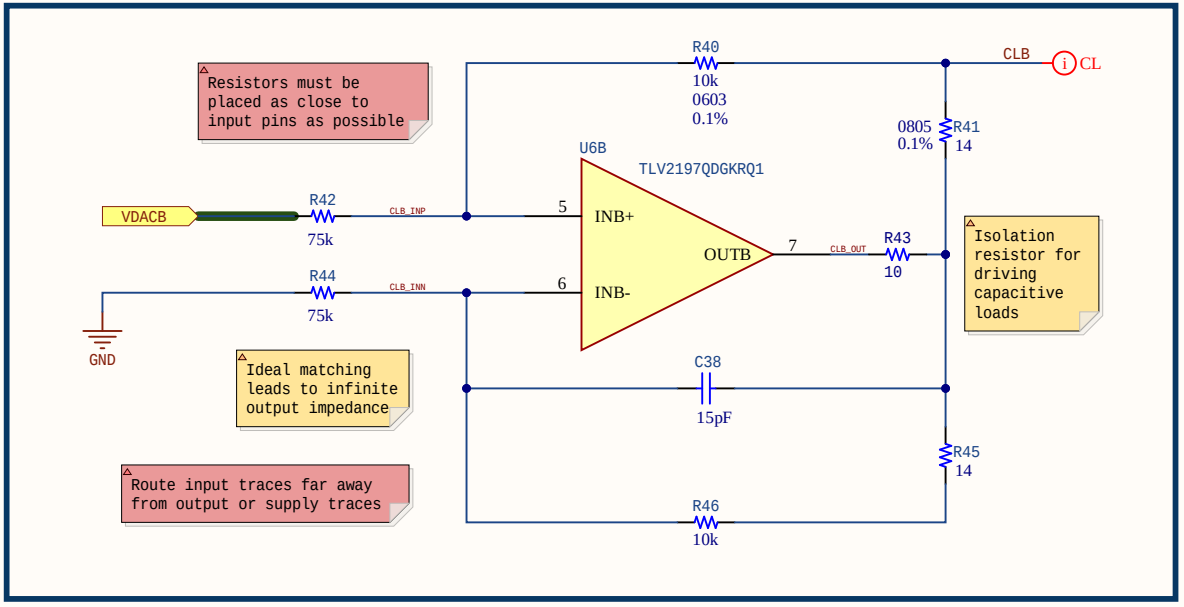
Settling time for VCL is 0.5ms after VDAC changes

SIG_P can be left floating. The current source on the SAM will get stuck at 24V

This is a Howland Current Pump. It takes the input voltage, VIN=(VIN+)−(VIN−), and forces a constant current through the load, set by VIN and the resistor ratio. Proper resistor matching ensures the output current is independent of load impedance.

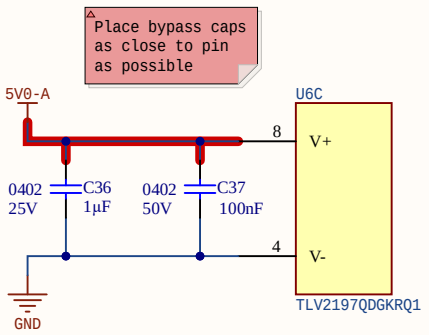
Signal I/O





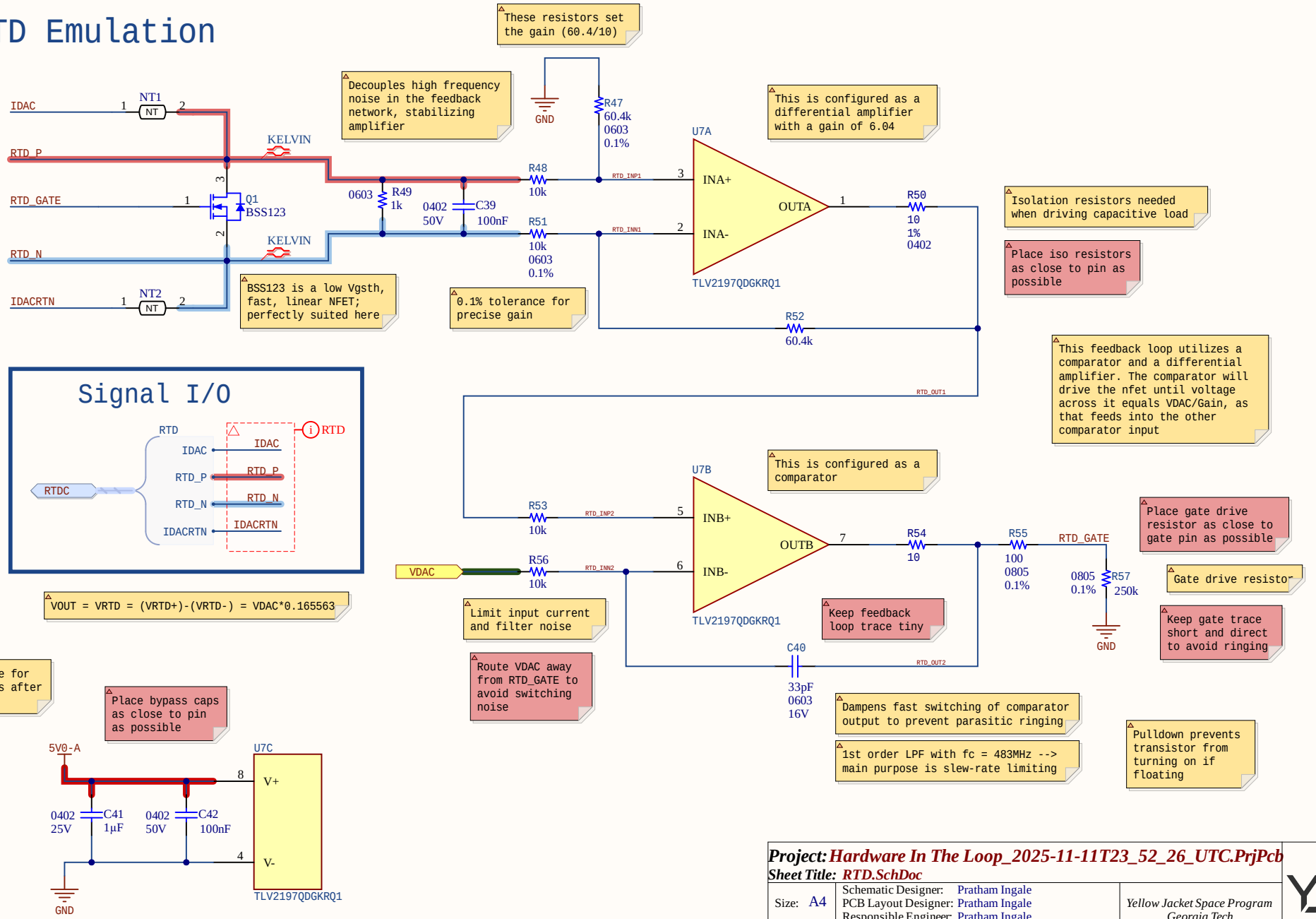
VSIG = (0.00953714*VDAC)*200

*FSAM & GSAMr4 are 100, but code multiplies by 2



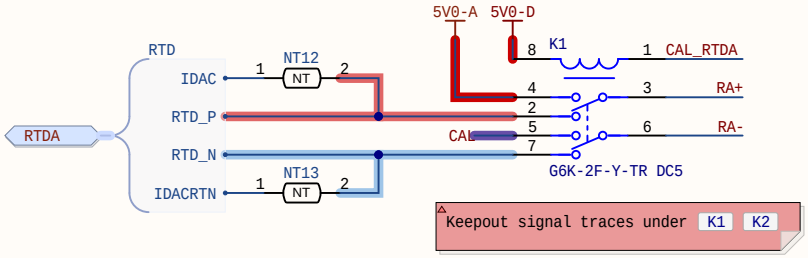
Project: *Hardware In The Loop_2025-11-11T23_52_26_UTC.PrjPcb*		
Sheet Title: *Current Loop.SchDoc*		
Size: A4	Schematic Designer: Pratham Ingale PCB Layout Designer: Pratham Ingale Responsible Engineer: Pratham Ingale	*Yellow Jacket Space Program* *Georgia Tech* *Atlanta, GA*
Date: 3/18/2026 Revision: 1.0 Sheet: 19 of: 28		

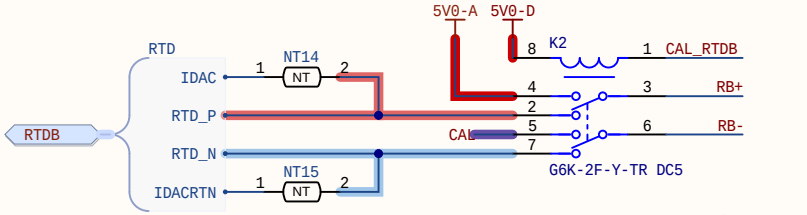
RTD Emulation

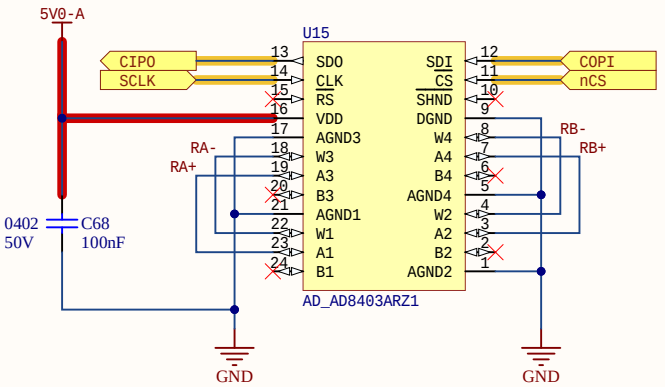


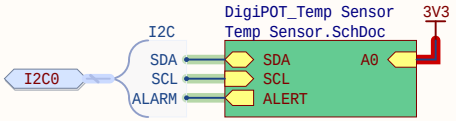
Project: *Hardware In The Loop_2025-11-11T23_52_26_UTC.PrjPcb*		
Sheet Title: *RTD.SchDoc*		
Size: A4	Schematic Designer: Pratham Ingale PCB Layout Designer: Pratham Ingale Responsible Engineer: Pratham Ingale	*Yellow Jacket Space Program* *Georgia Tech* *Atlanta, GA*
Date: 3/18/2026 Revision: 1.0 Sheet: 20 of: 28		

RTD Emulation

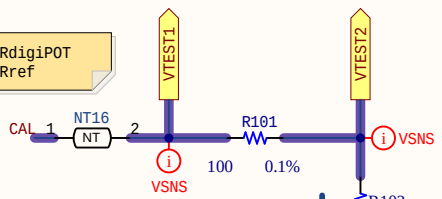








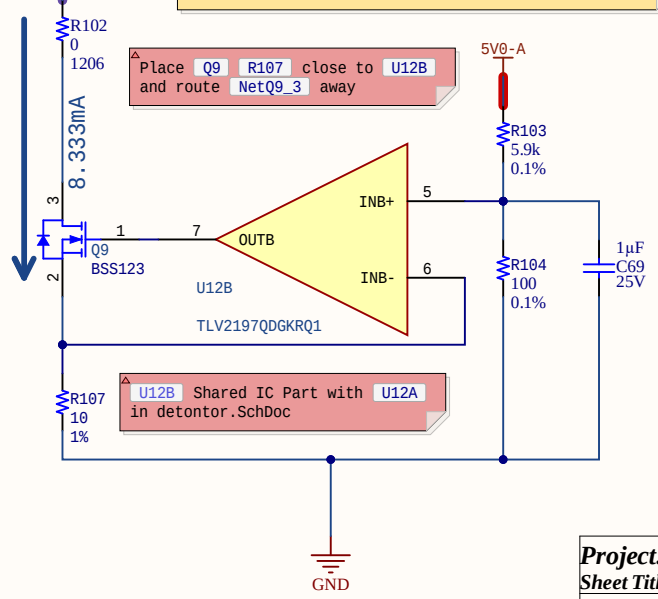
5V(FS) - VTEST1 = Iout * RdigiPOT
VTEST1 - VTEST2 = Iout * Rref



Iout = 5V * R103 / (R101 + R103) / 10 = 8.333mA
Rmax = 500R (digipot) + 100R (ref) = 5V / 8.333mA

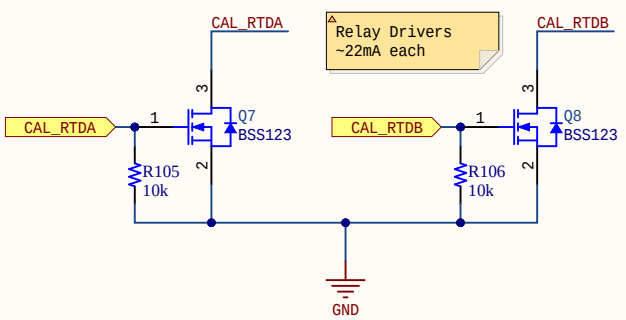
R102 Test Point for current calibration

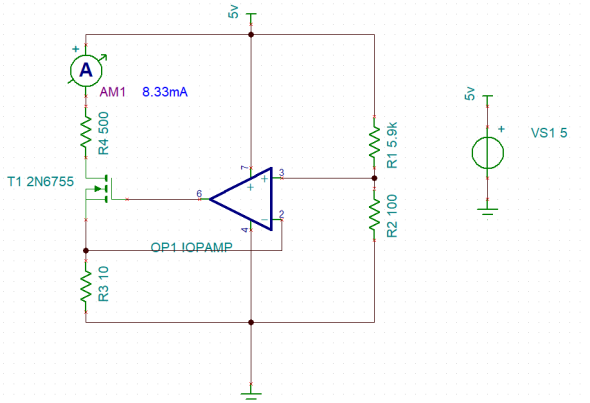
Place Q9 R107 close to U12B and route NetQ9_3 away



U12B Shared IC Part with U12A in detontor.SchDoc

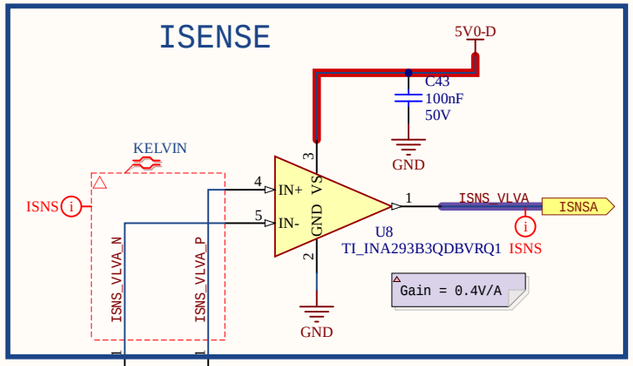
CAL_RTDA/RTDB: Only 1 can be open at a time!

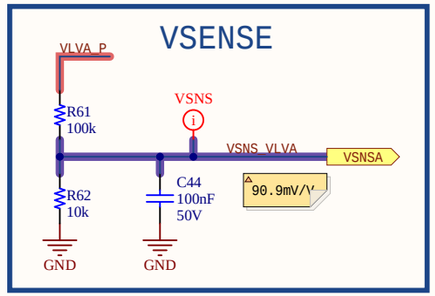


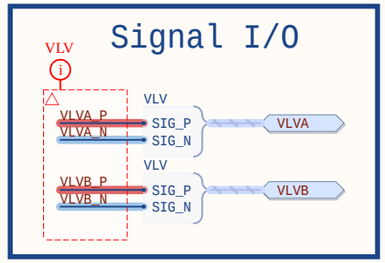


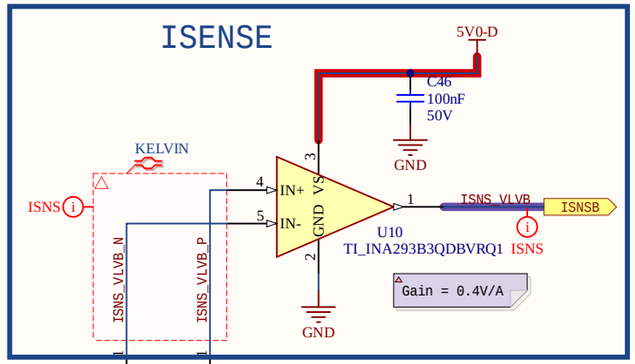
Project: *Hardware In The Loop_2025-11-11T23_52_26_UTC.PrjPcb*		
Sheet Title: *RTD DigiPOT.SchDoc*		
Size: A4	Schematic Designer: Peijie Liu PCB Layout Designer: Pratham Ingale Responsible Engineer: Pratham Ingale	*Yellow Jacket Space Program* *Georgia Tech* *Atlanta, GA*
Date: 3/18/2026 Revision: 1.0 Sheet: 21 of: 28		

Valve Emulation



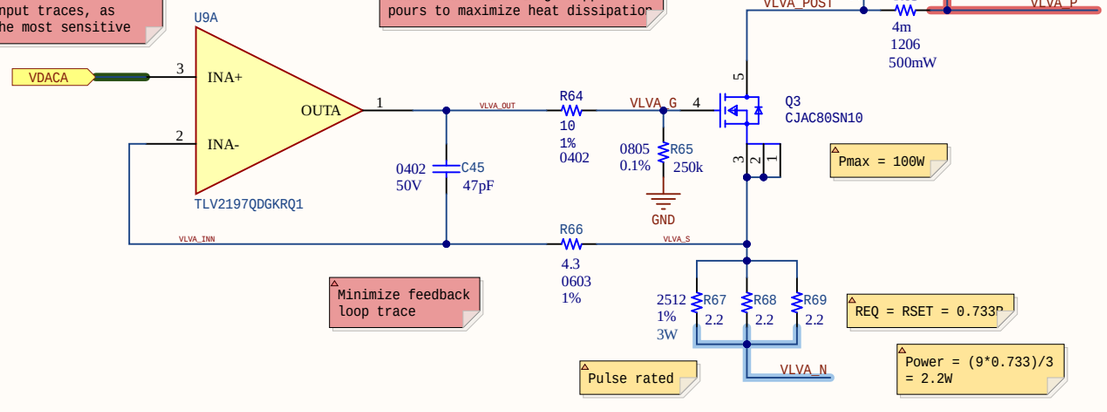






Minimize input traces, as they are the most sensitive

Route these with large copper pours to maximize heat dissipation



Pmax = 100W

Minimize feedback loop trace

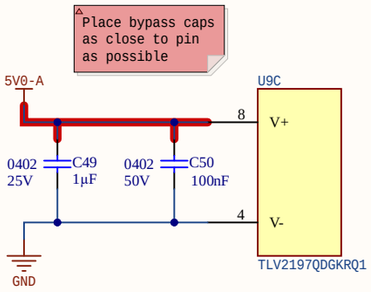
REQ = RSET = 0.733R

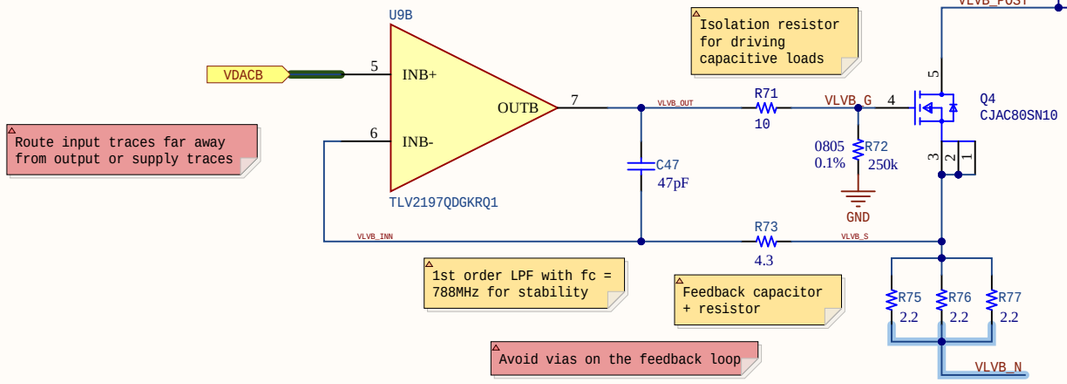
Power = (9*0.733)/3 = 2.2W

Pulse rated

IOUT = VDAC/RSET

This uses an op-amp to drive an NFET in its linear region, regulating current through RSET to match VDAC. The op-amp forms a closed feedback loop that adjusts the gate voltage to maintain IOUT = VDAC/RSET





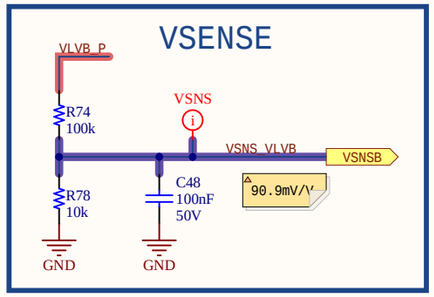
Isolation resistor for driving capacitive loads

Route input traces far away from output or supply traces

1st order LPF with fc = 788MHz for stability

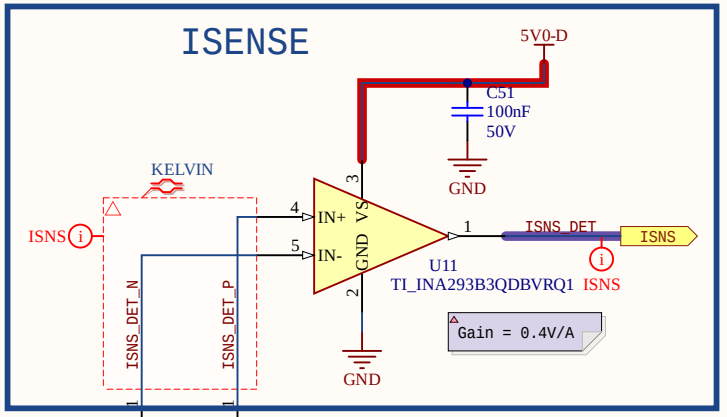
Feedback capacitor + resistor

Avoid vias on the feedback loop



Project: *Hardware In The Loop_2025-11-11T23_52_26_UTC.PrjPcb*		
Sheet Title: *Valve.SchDoc*		
Size: A4	Schematic Designer: Pratham Ingale PCB Layout Designer: Pratham Ingale Responsible Engineer: Pratham Ingale	*Yellow Jacket Space Program* *Georgia Tech* *Atlanta, GA*
Date: 3/18/2026 Revision: 1.0	Sheet: 22 of: 28	

Detonator Emulation



Route these with large copper pours to maximize heat dissipation

NT8 NT9

DET_POST_P

R79
4m
1206
500mW

DET_P

This uses an op-amp to drive an NFET in its linear region, regulating current through RSET to match VDAC. The op-amp forms a closed feedback loop that adjusts the gate voltage to maintain IOUT = VDAC/RSET

Minimize input traces, as they are the most sensitive

U12A

VDAC

INA+

INA-

OUTA

TLV2197QDGKRQ1

Isolation resistor for driving capacitive loads

DET_OUT

R80
10
1%
0402

DET_G

Q5
CJAC80SN10

0805
0.1%
R81
250k

GND

0402
50V
C52
47pF

1st order LPF with fc = 788MHz for stability

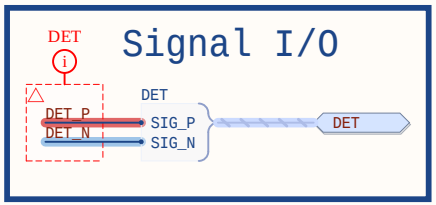
DET_INN

R82
4.3
0603
1%

DET_S

Pmax = 100W

IOUT = VDAC/RSET



R83 2.2
R84 2.2
R85 2.2
R86 2.2
R87 2.2
3W
2512

RSET = 2.2/5 = 0.44R

DET_N

PMAX = (5.7A*5.7A*0.44R) = 14.29W/5 = 2.86W

Place bypass caps as close to pin as possible

5V0-A

U12C

V+

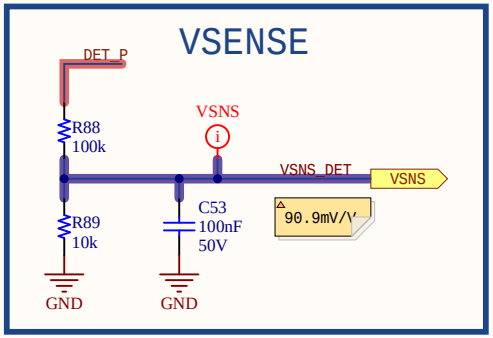
V-

TLV2197QDGKRQ1

0402
25V
C54
1µF

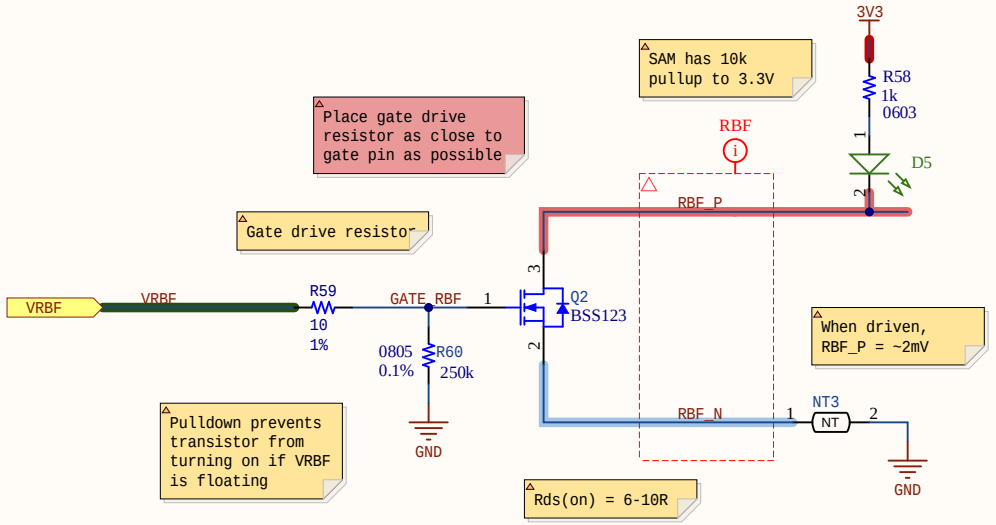
0402
50V
C55
100nF

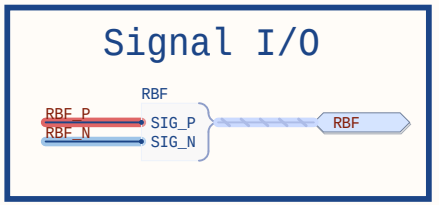
GND



Project: ***Hardware In The Loop_2025-11-11T23_52_26_UTC.PrjPcb***		
Sheet Title: ***Detonator.SchDoc***		
Size: A4	Schematic Designer: Pratham Ingale PCB Layout Designer: Pratham Ingale Responsible Engineer: Pratham Ingale	*Yellow Jacket Space Program* *Georgia Tech* *Atlanta, GA*
Date: 3/18/2026 Revision: 1.0	Sheet: 23 of: 28	

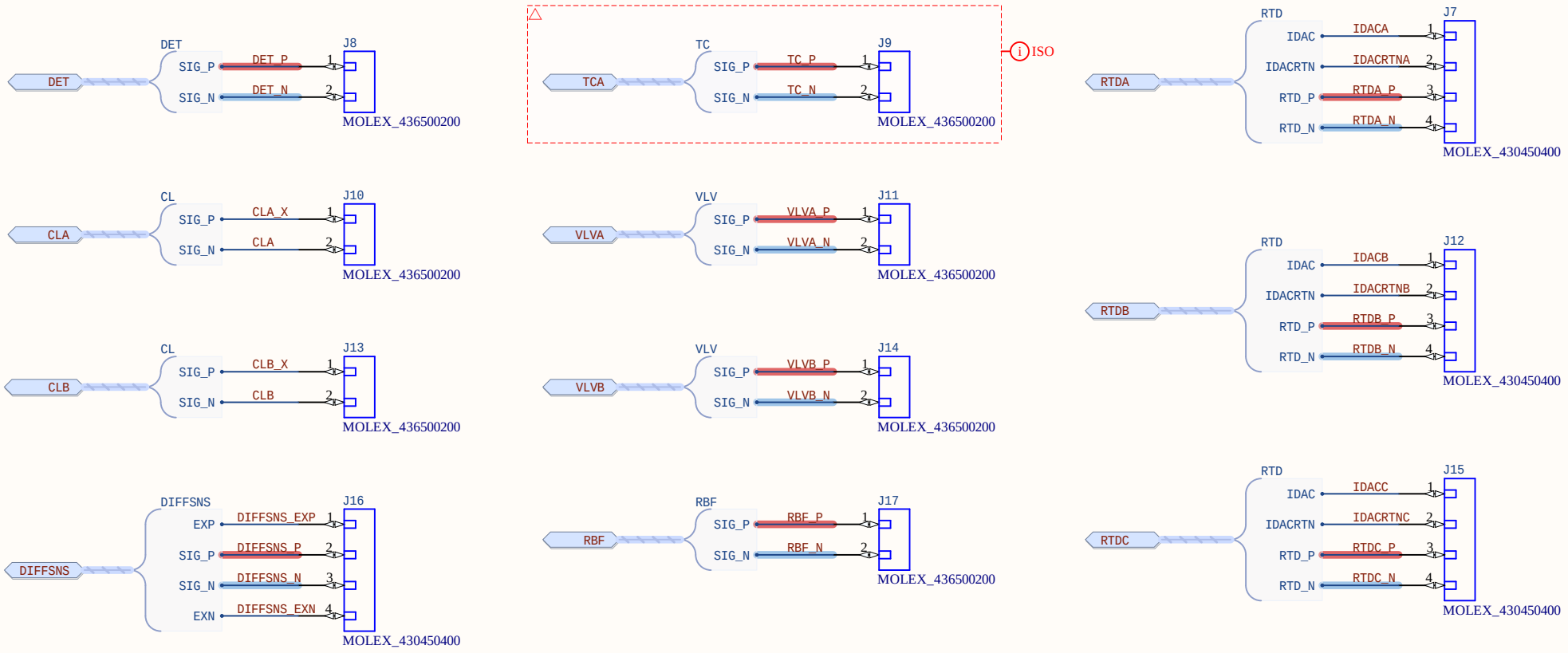
Remove Before Flight Tag Emulation



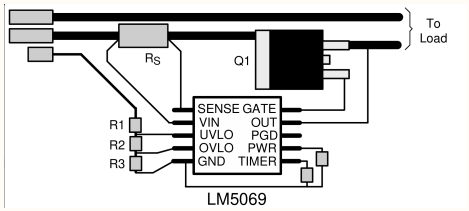


Project: *Hardware In The Loop_2025-11-11T23_52_26_UTC.PrjPcb*		
Sheet Title: *RBF Tag.SchDoc*		
Size: A4	Schematic Designer: Pratham Ingale PCB Layout Designer: Pratham Ingale Responsible Engineer: Pratham Ingale	*Yellow Jacket Space Program* *Georgia Tech* *Atlanta, GA*
Date: 3/18/2026 Revision: 1.0 Sheet: 24 of: 28		

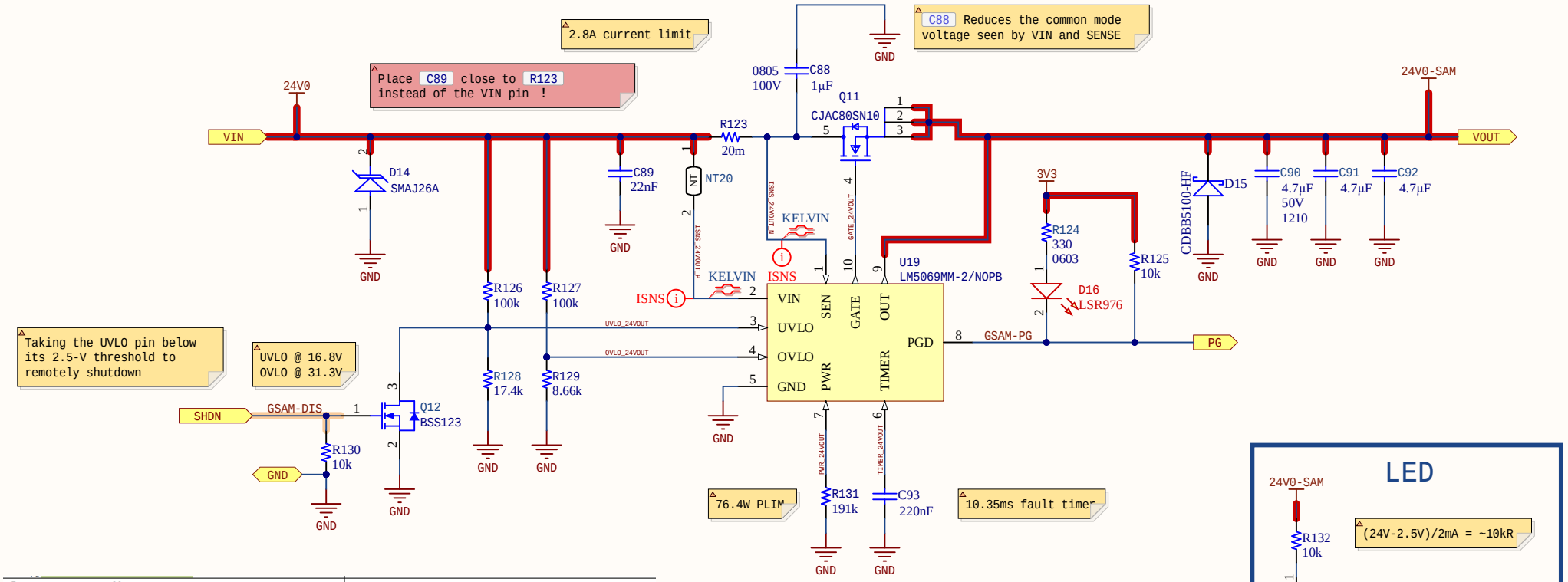
Signal Outputs



Project: *Hardware In The Loop_2025-11-11T23_52_26_UTC.PrjPcb*		
Sheet Title: *Sig Connectors.SchDoc*		
Size: A4	Schematic Designer: Pratham Ingale PCB Layout Designer: Pratham Ingale Responsible Engineer: Pratham Ingale	*Yellow Jacket Space Program* *Georgia Tech* *Atlanta, GA*
Date: 3/18/2026 Revision: 1.0 Sheet: 25 of: 28		



24V Output Load Switch



R_{SNS} =	20	mΩ
R_{CL1} =	DNP	Ω
R_{CL2} =	0	Ω
R_{PWR} =	191	kΩ
C_{TIMER} =	220.00	nF
R1 =	100	kΩ
R2 =	17.4	kΩ
R3 =	100	kΩ
R4 =	8.66	kΩ
C_{dvdt} =	DNP	nF
C_{IN} =	0.01	µF
D1	B380-13-F	
D2	DNP	
Q1	NON-TI MOSFET	
n parallel	1	
Q2	DNP	
Z1	5.0SMDxx	

Design Results

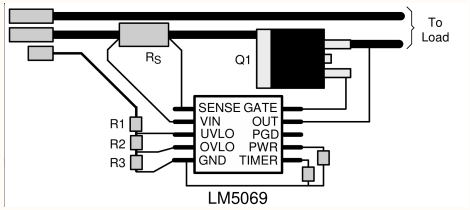
	Settings	Units
Current limit	2.8	A
Power Limit	76	W
Circuit Breaker Current	2.8	A
Startup Time	4.82	ms
Insertion Delay	160.0	ms
Fault Timeout	10.35	ms
Restart Time During Fault	2069.424	ms
Upper UVLO Threshold	18.968	V
Lower UVLO Threshold	16.868	V
Upper OVLO Threshold	31.368	V
Lower OVLO Threshold	29.268	V

LED

Project: *Hardware In The Loop_2025-11-11T23_52_26_UTC.PrjPcb*
Sheet Title: *24V Output Load Switch.SchDoc*

Size: A4	Schematic Designer: Peijie Liu PCB Layout Designer: Pratham Ingale Responsible Engineer: Pratham Ingale	*Yellow Jacket Space Program* *Georgia Tech* *Atlanta, GA*
Date: 3/18/2026 Revision: 1.0 Sheet: 26 of: 28		

48V Output Load Switch



1.5A current limit

C94 Reduces the common mode voltage seen by VIN and SENSE

Place C95 close to R133 instead of the VIN pin !

48V0 VIN D19 SMAJ51A R133 40m NT NT21 C95 22nF C94 0805 100V 1µF Q13 CJAC80SN10 48V0-SAM 48V VOUT D18 CDBB5100-HF C96 10µF 100V 1210 C97 10µF GND

KELVIN ISNS 48V ISNS_48VOUT_P ISNS_48VOUT_N GATE_48VOUT

3V3 R134 330 0603 D20 LSR976 R135 10k

U20 LM5069MM-2/NOPB
VIN SEN GATE OUT UVLO PGD OVLO PWR GND TIMER

R136 191k R137 191k R138 14.7k R139 8.66k

UVLO @ 35.0V
OVLO @ 57.6V

UVLO_48VOUT OVLO_48VOUT

FSAM-PG PG

SHDN FSAM-DIS Q14 BSS123 R140 10k

Taking the UVLO pin below its 2.5-V threshold to remotely shutdown

42W PLIM

PWR_48VOUT TIMER_48VOUT R141 191k C98 470nF

22.12ms fault time

LED

48V0-SAM R142 17.4k D21 LGR971-KN-1 GND

(48V-2.5V)/17.5kR = 2.6mA

R_{SNS} =	36	mΩ
R_{CL1} =	DNP	Ω
R_{CL2} =	0	Ω
R_{PWR} =	191	kΩ
C_{TIMER} =	470.00	nF
R1 =	191	kΩ
R2 =	14.7	kΩ
R3 =	191	kΩ
R4 =	8.66	kΩ
C_{dvdt} =	DNP	nF
C_{IN} =	0.01	µF
D1	B380-13-F	
D2	DNP	
Q1	NON-TI MOSFET	
#FETs in parallel	1	
Q2	DNP	
Z1	5.0SMDxx	

red when t start-up

: C_{dvdt}

Design Results

	Settings	Units
Current limit	1.5	A
Power Limit	42	W
Circuit Breaker Current	1.5	A
Startup Time	10.97	ms
Insertion Delay	341.8	ms
Fault Timeout	22.12	ms
Restart Time During Fault	4421.041	ms
Upper UVLO Threshold	38.994	V
Lower UVLO Threshold	34.983	V
Upper OVLO Threshold	57.639	V
Lower OVLO Threshold	53.628	V

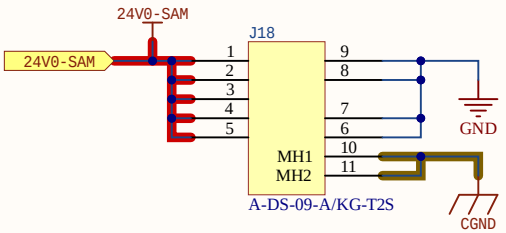
Ignore the 36mohm in this screenshot, it was needed to make the calculator work

Project: *Hardware In The Loop_2025-11-11T23_52_26_UTC.PrjPcb*
Sheet Title: *48V Output Load Switch.SchDoc*

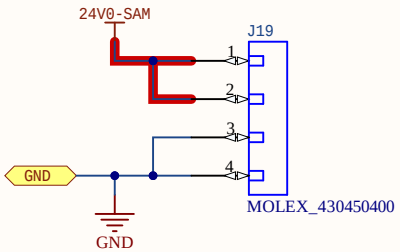
Size: A4	Schematic Designer: Peijie Liu PCB Layout Designer: Pratham Ingale Responsible Engineer: Pratham Ingale	*Yellow Jacket Space Program* *Georgia Tech* *Atlanta, GA*
Date: 3/18/2026 Revision: 1.0 Sheet: 27 of: 28		

Power Output

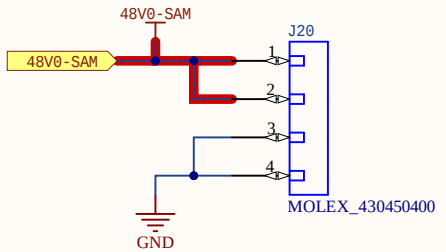
SAM5 Power



GSAM Power



FSAM Power



Project: *Hardware In The Loop_2025-11-11T23_52_26_UTC.PrjPcb*		
Sheet Title: *Output Power.SchDoc*		
Size: A4	Schematic Designer: Pratham Ingale PCB Layout Designer: Pratham Ingale Responsible Engineer: Pratham Ingale	*Yellow Jacket Space Program* *Georgia Tech* *Atlanta, GA*
Date: 3/18/2026 Revision: 1.0 Sheet: 28 of: 28		